

MODEL NAME :ZAW12

PCB NO : LA-A691P

BOM P/N : DA60012B000 LA-A691P M/B

DA40001G410 LS-9105P POWER BUTTON/B

DA40001FP10 LS-9102P USB/B

DA40001FQ10 LS-9103P TP BUTTON/B

DA40001FR10 LS-9104P ODD/B

Dell / Compal Confidential

Schematic Document

AMD FP2 Richland Processor with DDRIII + Bolton M3 FCH

AMD VGA Sun XT

2013-05-23

Rev: 1.0

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

UMA@ : Only for UMA

DIS@ : Only for Discrete

GCLK@ : Green CLK implemented

NGCLK@ : Non Green CLK implemented

@3221: ALC 3221

@3223 : ALC 3223

EMC@ : EMC Parts

NEMC@ : EMC不上件

R1@ : R1 P/N for PCB

R3@ : R3 P/N for PCB

THR1@ : Thames-XT R1 P/N

THR3@ : Thames-XT R3 P/N

CHR1@ : Chelsea-Pro R1 P/N

CHR3@ : Chelsea-Pro R3 P/N

R@ : RTD2132-R

S@ : RTD2132-S

KBBL@ : KeyBoard Backlight

X76@ : VRAM Group

CH@ : Chelsea M2

SE@ : Seymour M2

TH@ : Thames-XT

Mars@ : Mars Pro M2

A4R1@ : A4 APU-R1

A6R1@ : A6 APU-R1

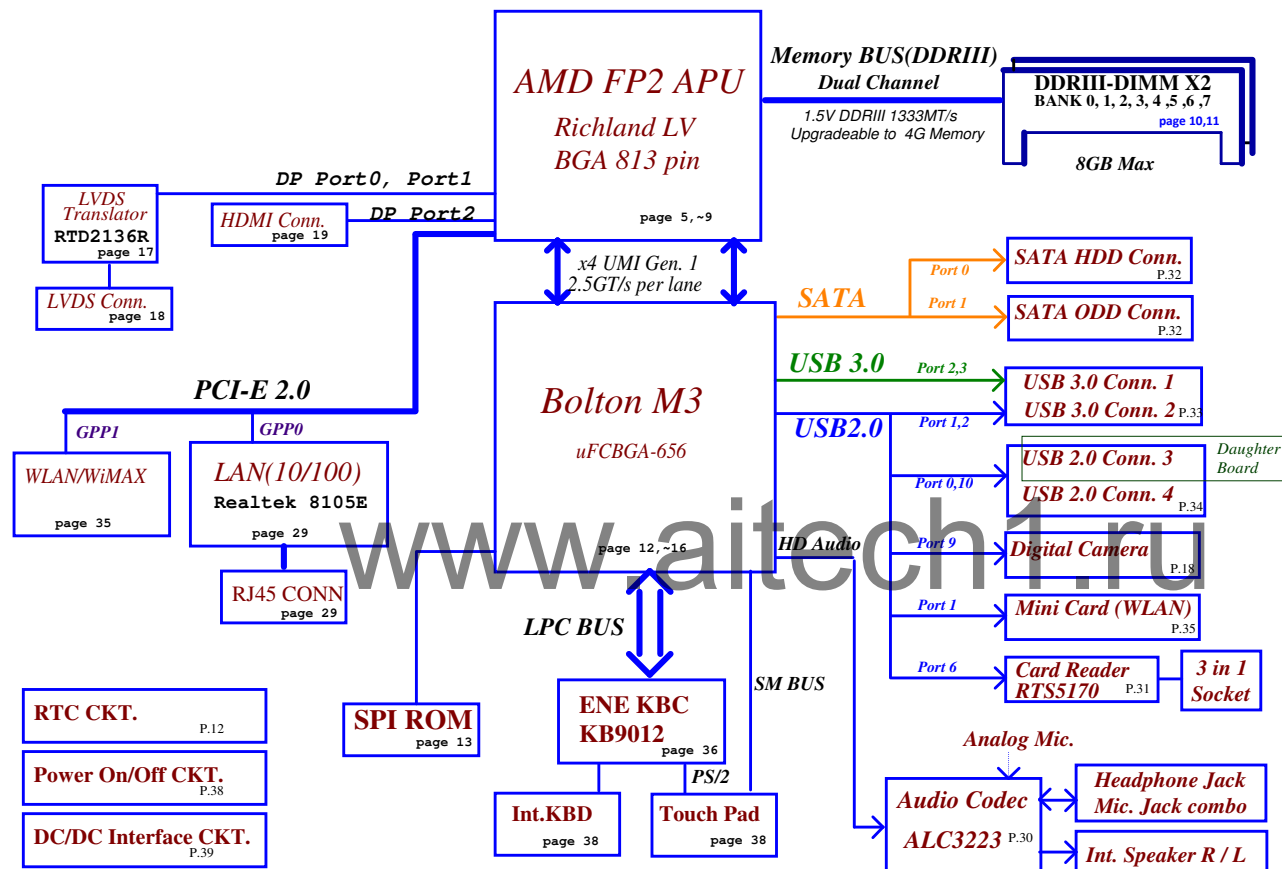
A8R1@ : A8 APU-R1

A8@ : A8 APU Symbol

Hud@ : HUDSON-M3

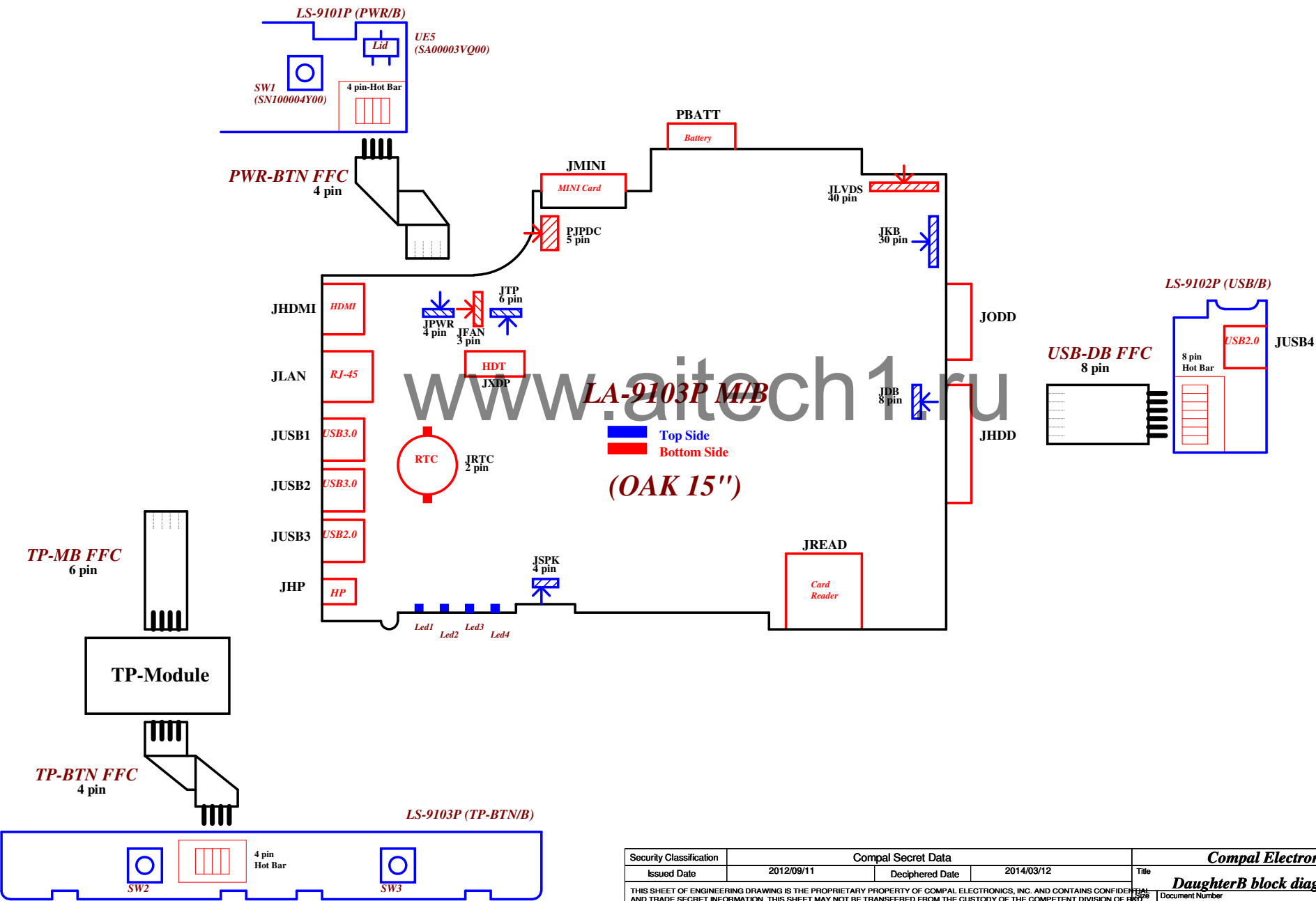
Bol@ : BOLTON-M3

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				LA-9103P
				Date: Wednesday, July 10, 2013
				Sheet 1 of 52
				Rev 1.0



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Project Code : VAW03
File Name : LA-9103P



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0 SD028330280
4	
5	
6	
7	

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	000 1011	11h 0x16	ADM1032ARMZ	100 1101	4Dh 0x9A
Charger IC	000 1001	09h 0x12	SB-TSI	100 1100	4Ch 0x98
			RTD2132	100 1010	4Ah 0x94
			GPU	100 0001	41h 0x82

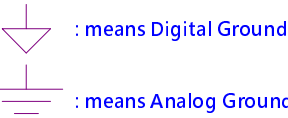
SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

Symbol Note :



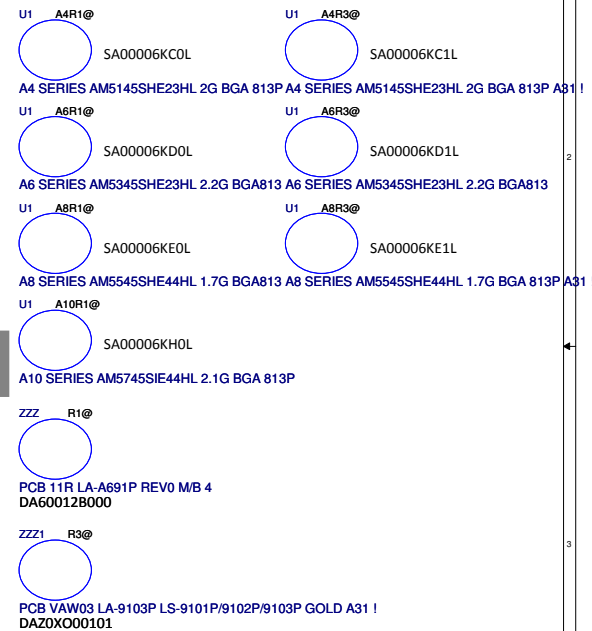
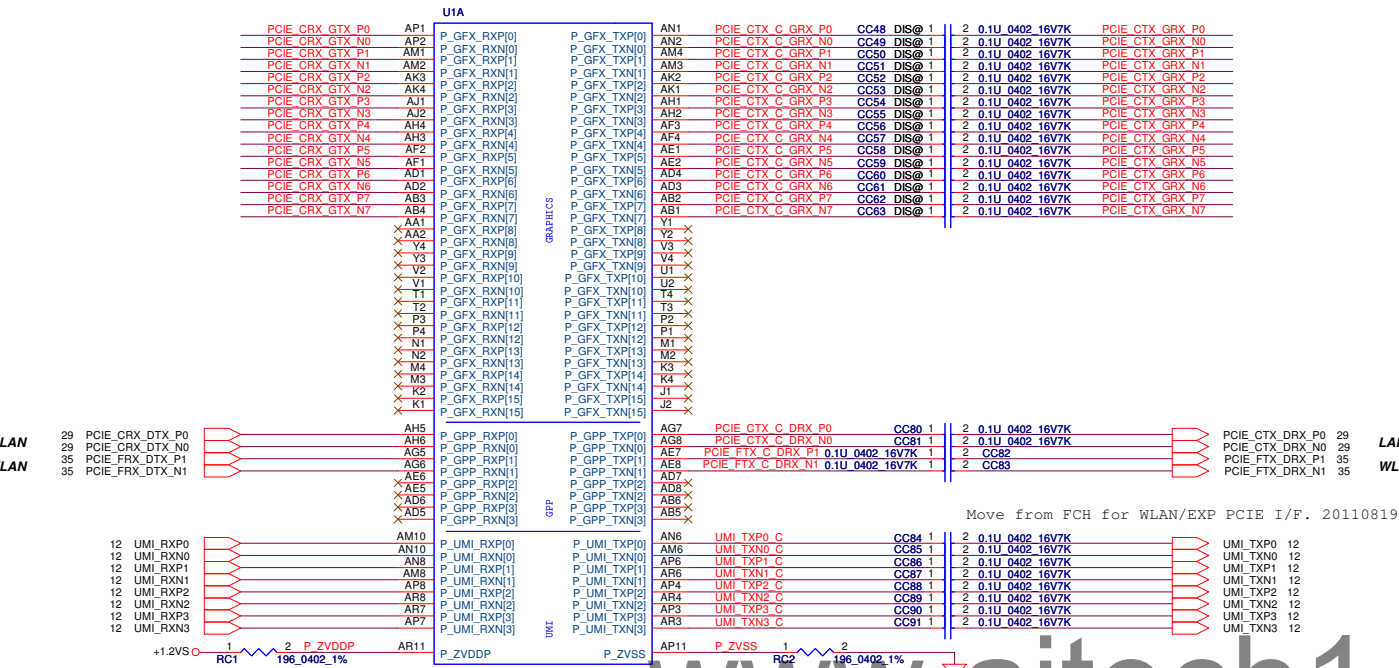
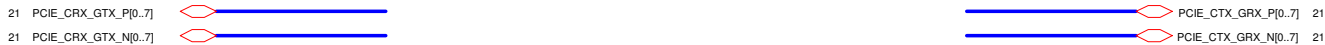
FCH

USB PORT#	DESTINATION
0	USB conn.3 DEBUG PORT
1	MINI CARD (WLAN)
2	USB conn.4
3	NC
4	NC
5	NC
6	Card Reader
7	NC
8	NC
9	Camera
10	USB conn.2
11	NC
12	NC
13	USB conn.1

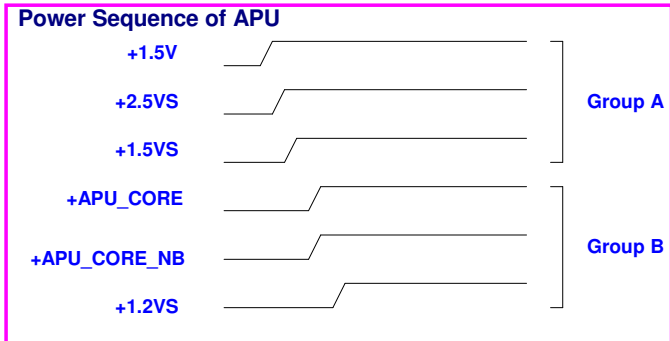
CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	None
	CLKOUT_PCIE1	None
	CLKOUT_PCIE2	10/100 LAN
	CLKOUT_PCIE3	MINI CARD WLAN
	CLKOUT_PCIE4	None
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
	CLKOUT_PEG_B	None

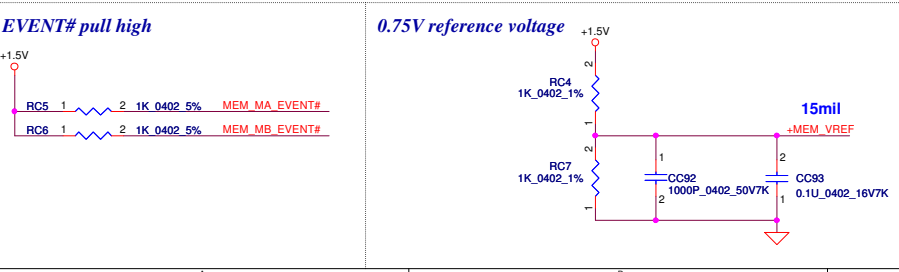
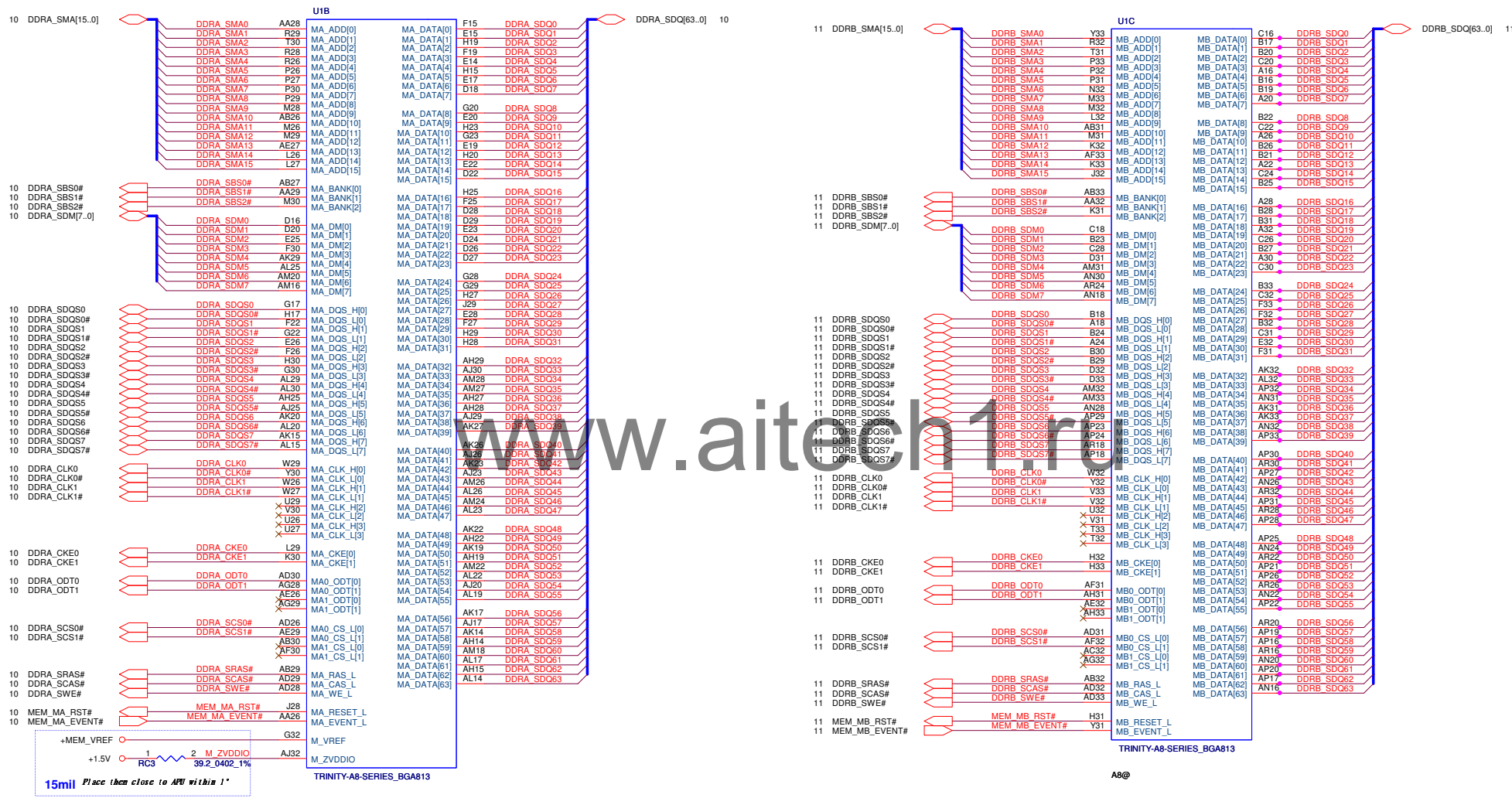
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



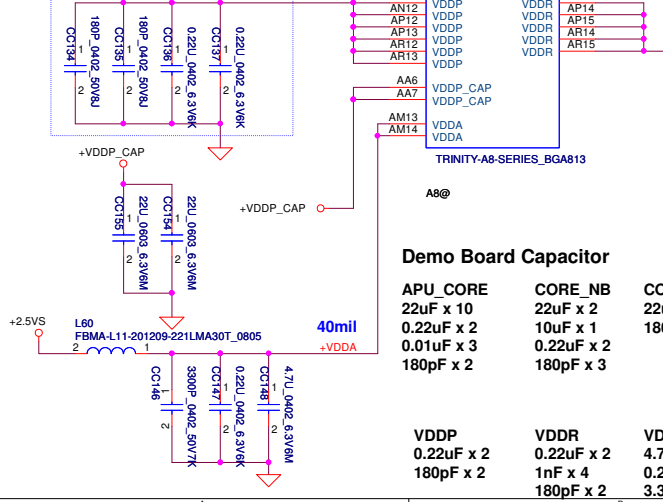
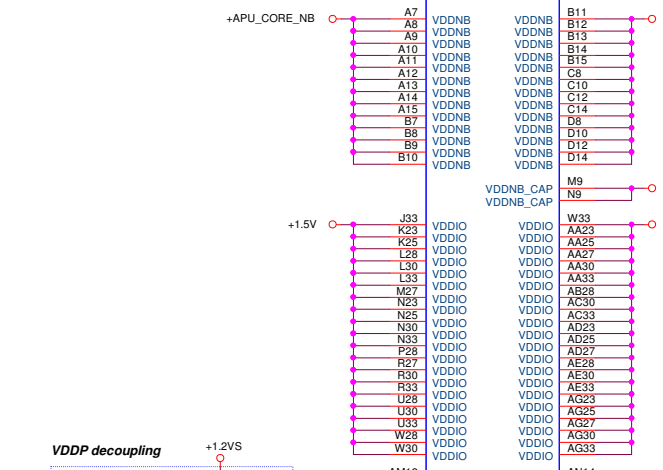
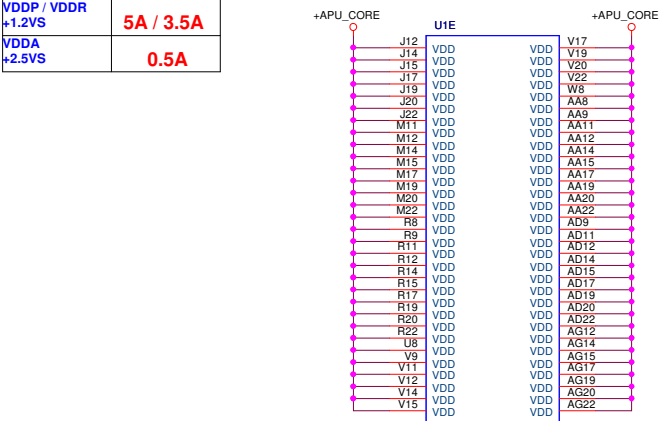
Item	Material P/N	Model DELL PN	Description	Vendor Contact Window
A4-5145M_Dual-Core,FP2(Group B),17W,Richland APU R1_ROH(Production)_HD 8310G	SA00006KC0L	VAW03	S IC A4 SERIES AM5145SHE23HL 2G BGA 813P	AMD
A4-5145M_Dual-Core,FP2(Group B),17W,Richland APU R3_ROH(Production)_HD 8310G	SA00006KC1L	8C6MV	S IC A4 SERIES AM5145SHE23HL 2G BGA 813P A31 I	AMD
A6-5345M_Dual-Core,FP2(Group B),17W,Richland APU R1_ROH(Production)_HD 8410G	SA00006KD0L	VAW03	S IC A6 SERIES AM5345SHE23HL 2.2G BGA 813P	AMD
A6-5345M_Dual-Core,FP2(Group B),17W,Richland APU R3_ROH(Production)_HD 8410G	SA00006KD1L	VGDH2	S IC A6 SERIES AM5345SHE23HL 2.2G BGA 813P A31 I	AMD
A8-5545M_Quad-Core,FP2(Group B),19W,Richland APU R1_ROH(Production)_HD 8510G	SA00006KE0L	VAW03	S IC A8 SERIES AM5545SHE44HL 1.7G BGA 813P	AMD
A8-5545M_Quad-Core,FP2(Group B),19W,Richland APU R3_ROH(Production)_HD 8510G	SA00006KE1L	Y53MJ	S IC A8 SERIES AM5545SHE44HL 1.7G BGA 813P A31 I	AMD
A10-5745M_Quad-Core,FP2(Group B),25W,Richland APU R1_ROH(Production)_HD 8610G	SA00006KH0L	VAW03	S IC A10 SERIES AM5745SIE44HL 2.1G BGA 813P	AMD
A10-5745M_Quad-Core,FP2(Group B),25W,Richland APU R3_ROH(Production)_HD 8610G		缺 DPN		AMD





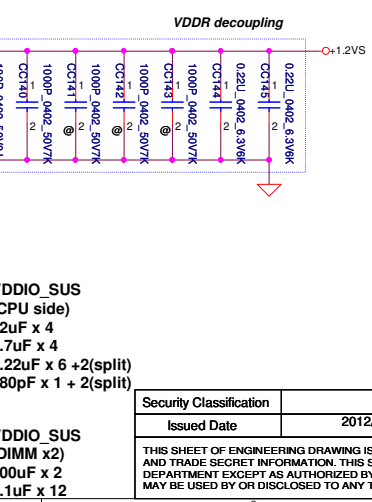
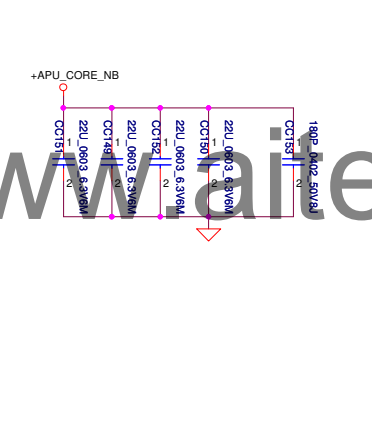
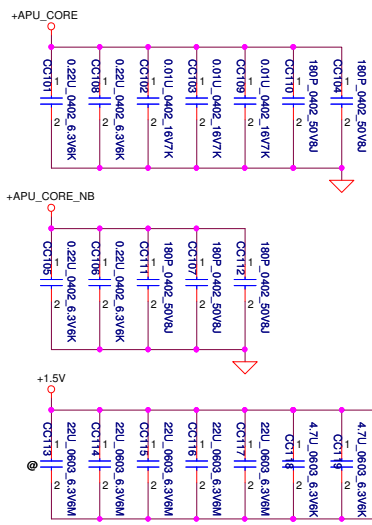
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	FP2 DDRIII Memory I/F
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				Date	Wednesday, July 10, 2013
				Sheet	6 of 52
				Rev	1.0

Power Name	Consumption
VDD	
+APU_CORE	60A
VDDNB	
+APU_CORE_NB	29A
VDDIO	
+1.5V	3.2A
VDDP / VDDR	
+1.2VS	5A / 3.5A
VDDA	
+2.5VS	0.5A



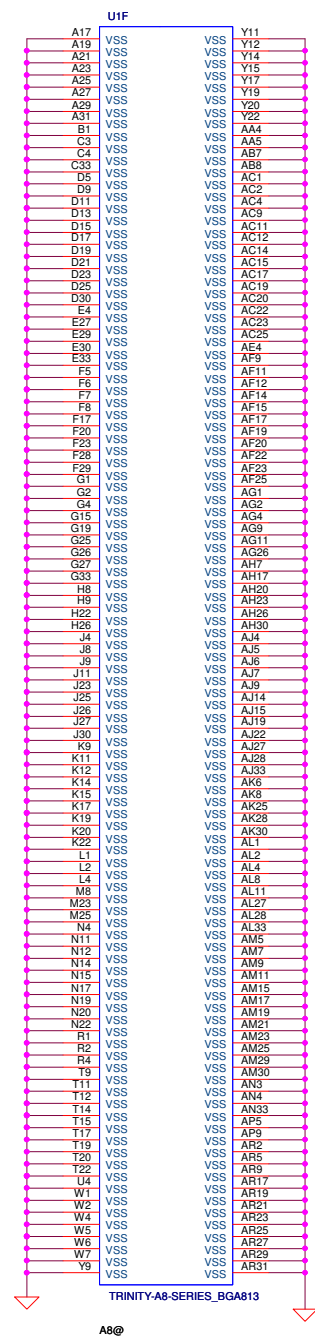
Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	22uF x 4	22uF x 4
0.01uF x 3	0.22uF x 2	4.7uF x 4	0.22uF x 6 +2(split)
180pF x 2	180pF x 3	180pF x 1	180pF x 1 + 2(split)
VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

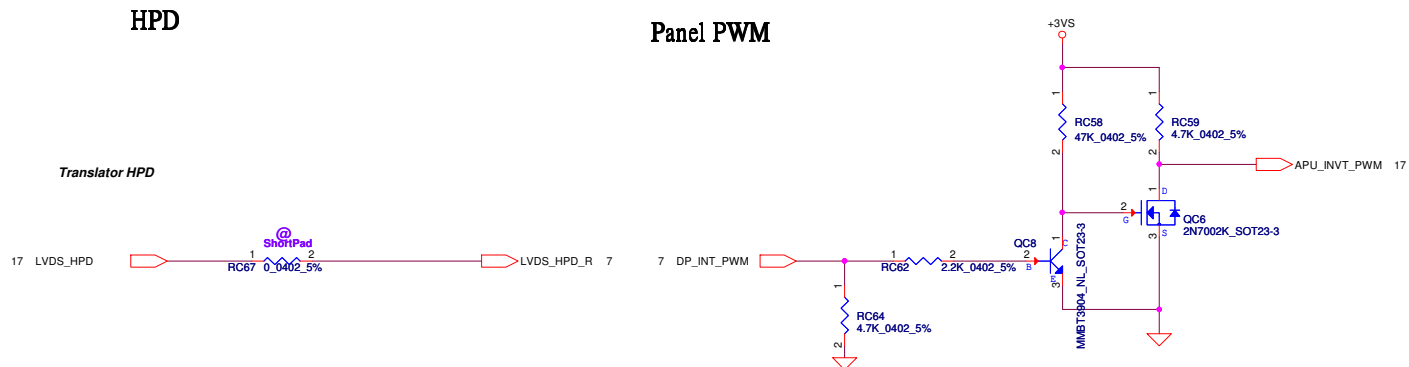


across VDDIO and VSS split

$$(330\mu F \cdot 6.3V \cdot 4.2L \cdot ESR17m) \cdot *1 = (SF000002Z00)$$

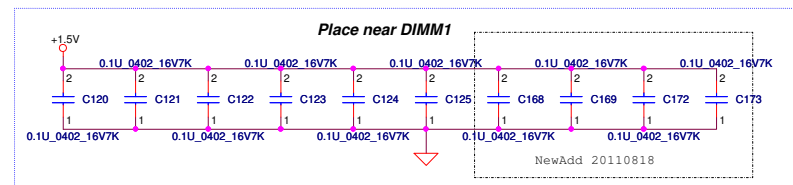


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								Document Number		LA-9103P		Rev	
								Date		Wednesday, July 10, 2013		Sheet	
								8		of 52			

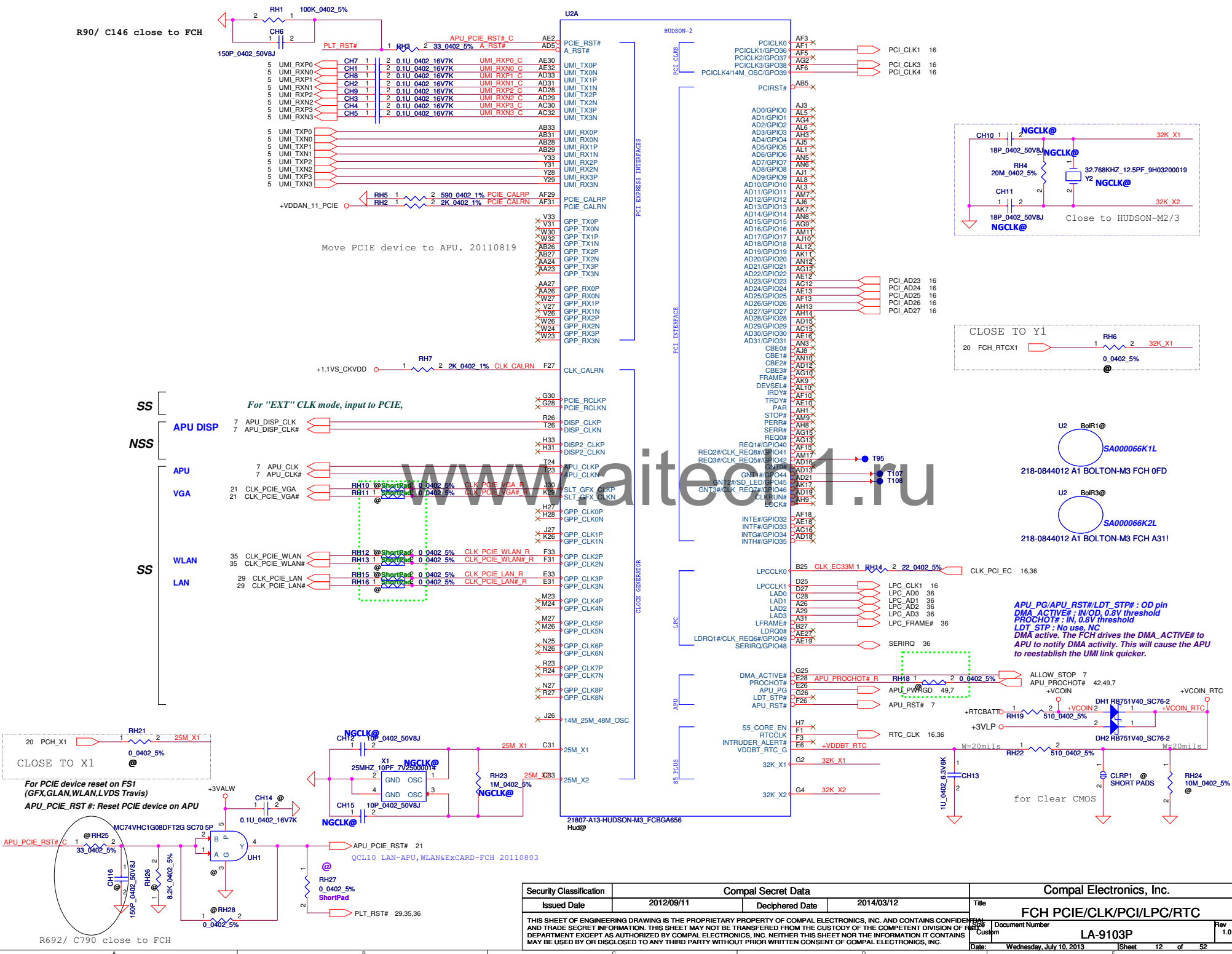


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				Date	Wednesday, July 10, 2013
				Sheet	9 of 52
				Rev	1.0

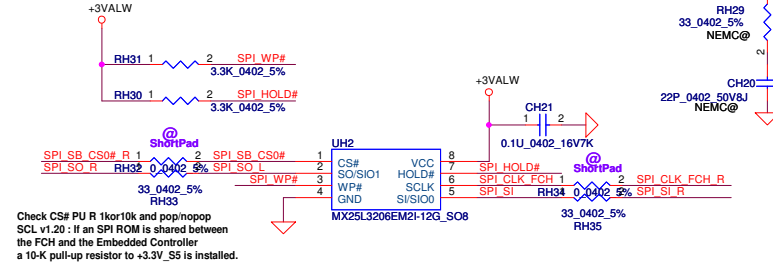
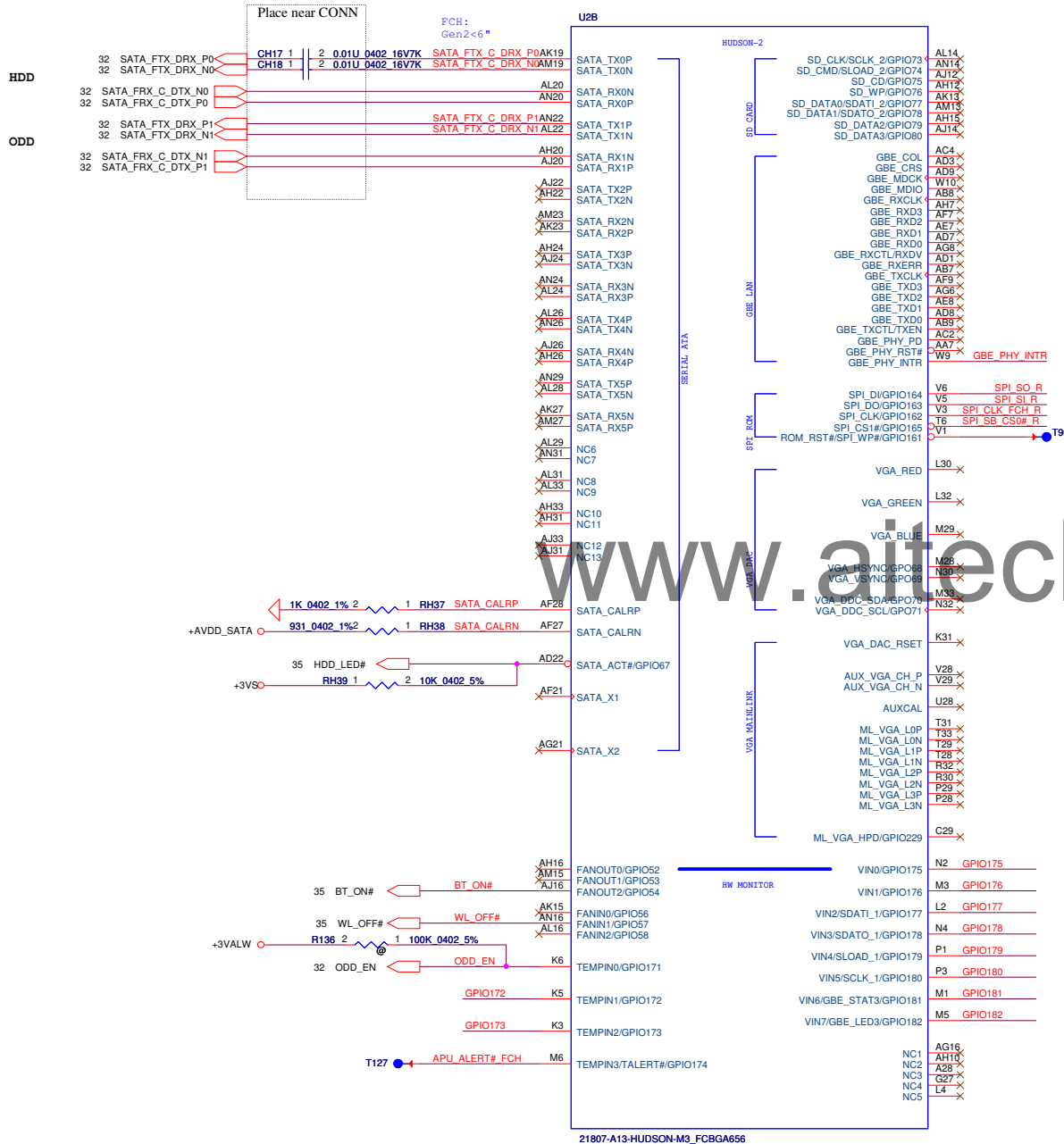


Reverse H:4mm
<Address: 00>



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				Customer	LA-9103P	1.0
Date: Wednesday, July 10, 2013				Sheet	12	of 52

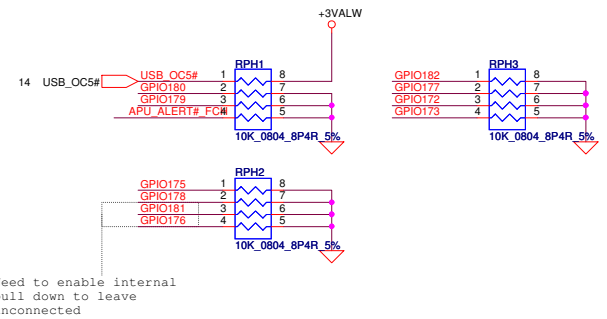
4MB SPI ROM & Non-share ROM.



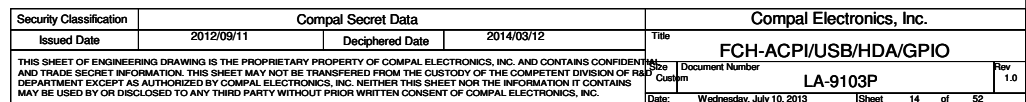
GBE_PHY_INTR
 Pulled-up to +3.3V_S5 with a 10-K 5% resistor.
 FCH SCL v1.20 #19-85

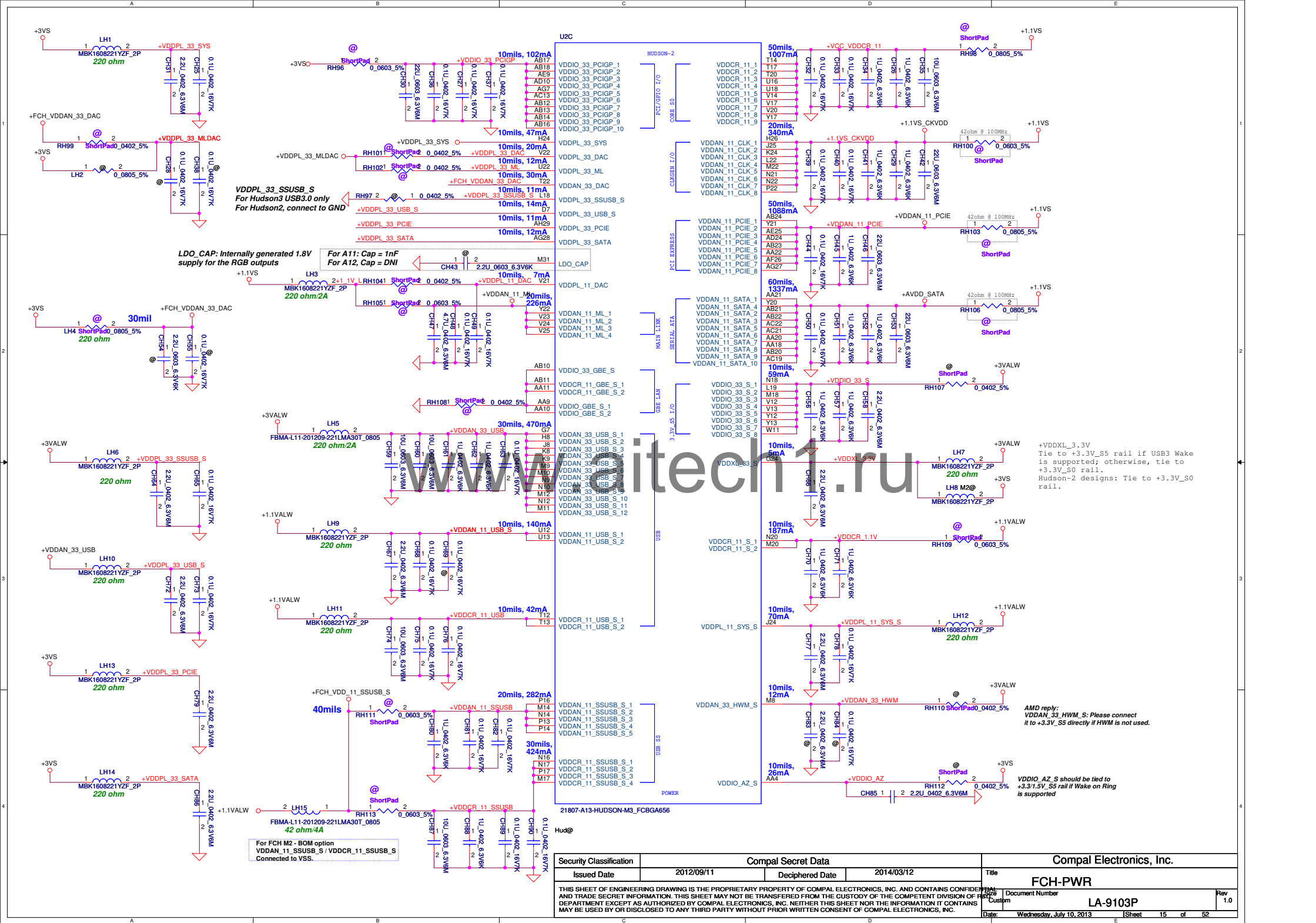
GBE_PHY_INTR RH36 1 2 10K 0402 5%

Removed RGMII/MII support and updated termination requirements for GBE_COL, GBE_CRS, GBE_RXERR and GBE_MDIO when RGMII/MII interface is not used.
 FCH DGv1.20 / SCL v1.20



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								LA-9103P		1.0	
								Date: Wednesday, July 10, 2013		Sheet 13 of 52	



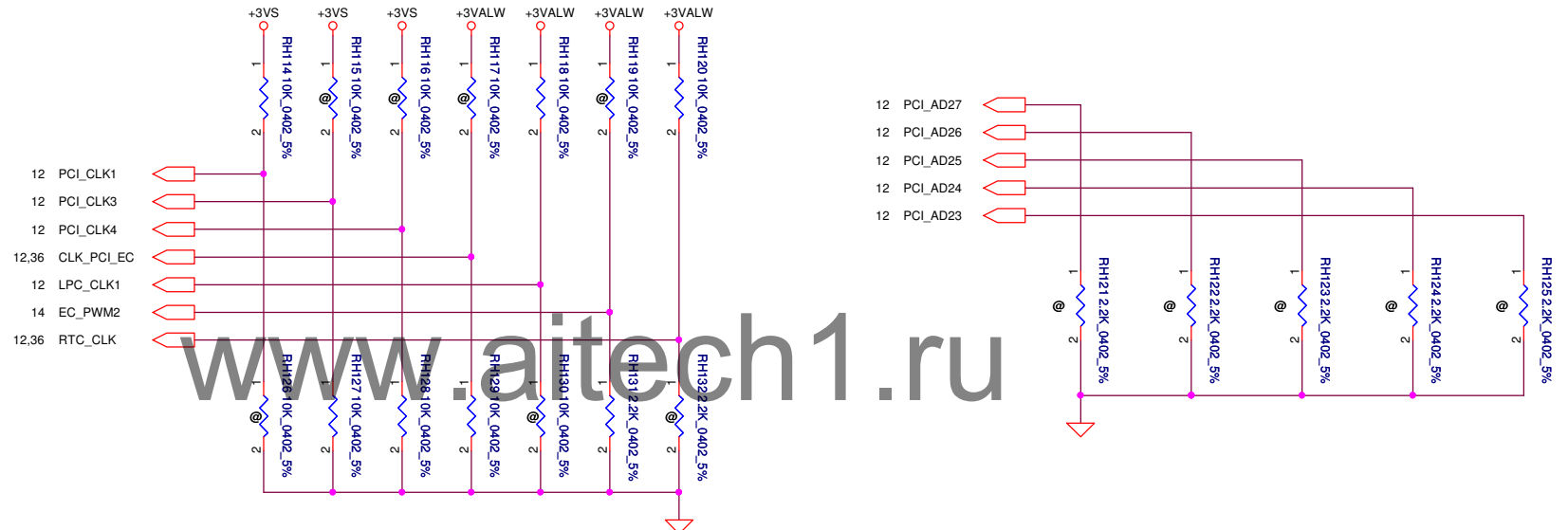


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Date: Wednesday, July 10, 2013				Sheet	15	of 52

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

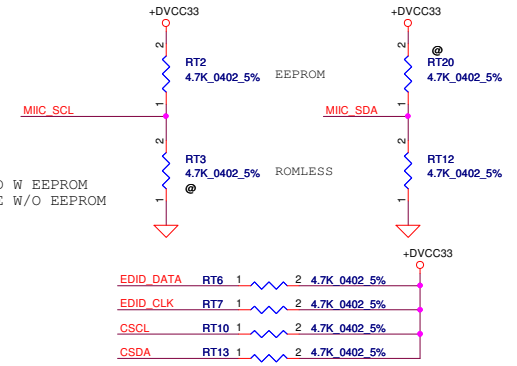
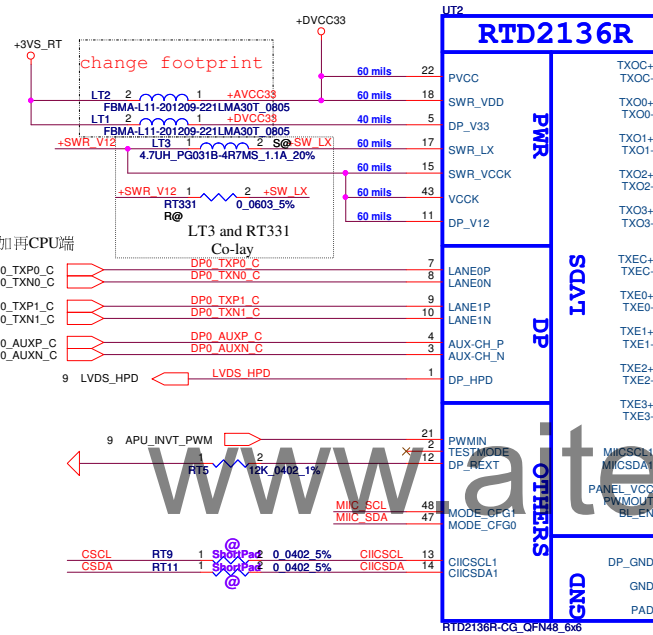
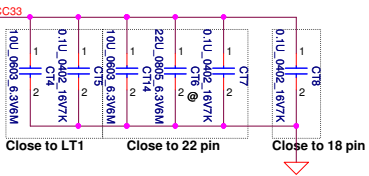
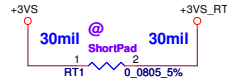
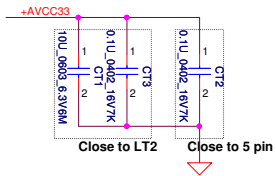
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

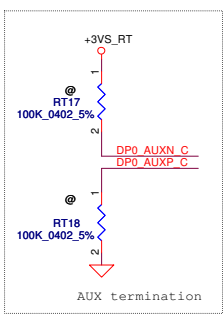
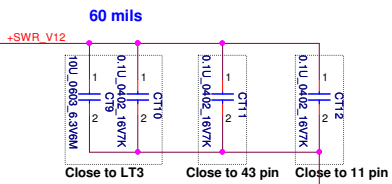
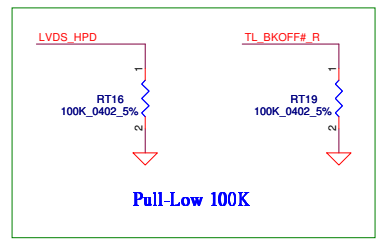


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				LA-9103P		
Date: Wednesday, July 10, 2013				Sheet	16	of 52

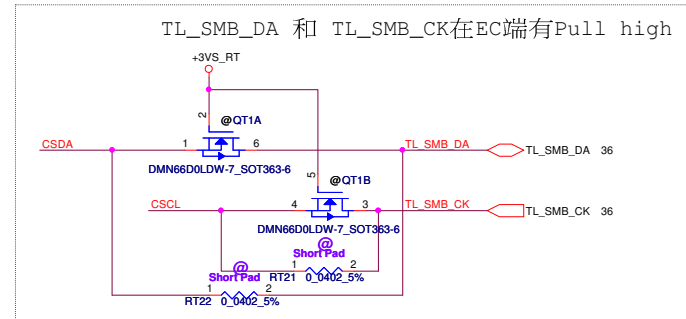
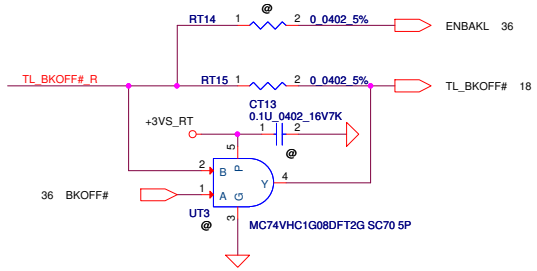
Pin22 (DPV33) < 20mA
Pin 11 (DP_V12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA



		Pin47 MIIC_SDA	
		0	1
Pin48 MIIC_SCL	0	x	EP MODE
	1	ROM	EEPROM

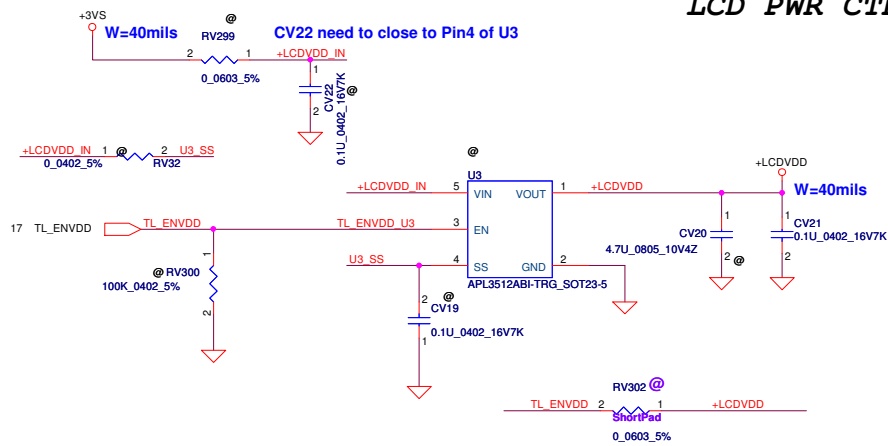


Vendor advise reserve it

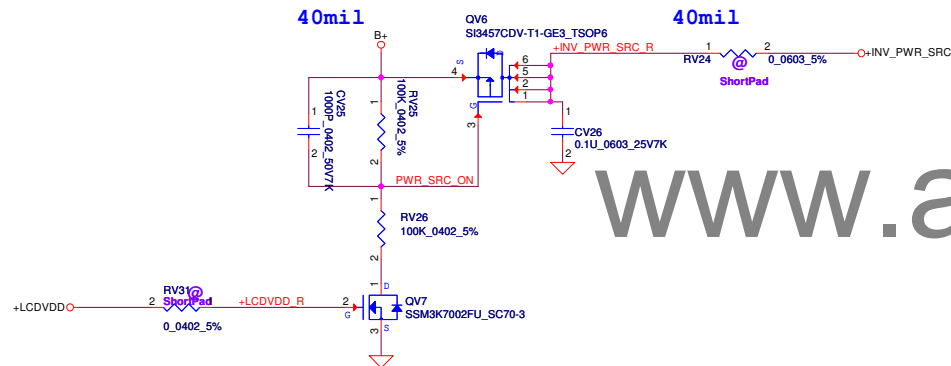


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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	LVDS Translator - RTD2132R	
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				Date	Wednesday, July 10, 2013	Sheet 17 of 52

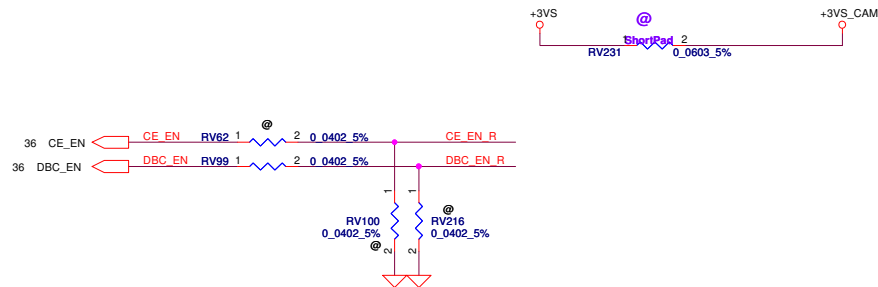
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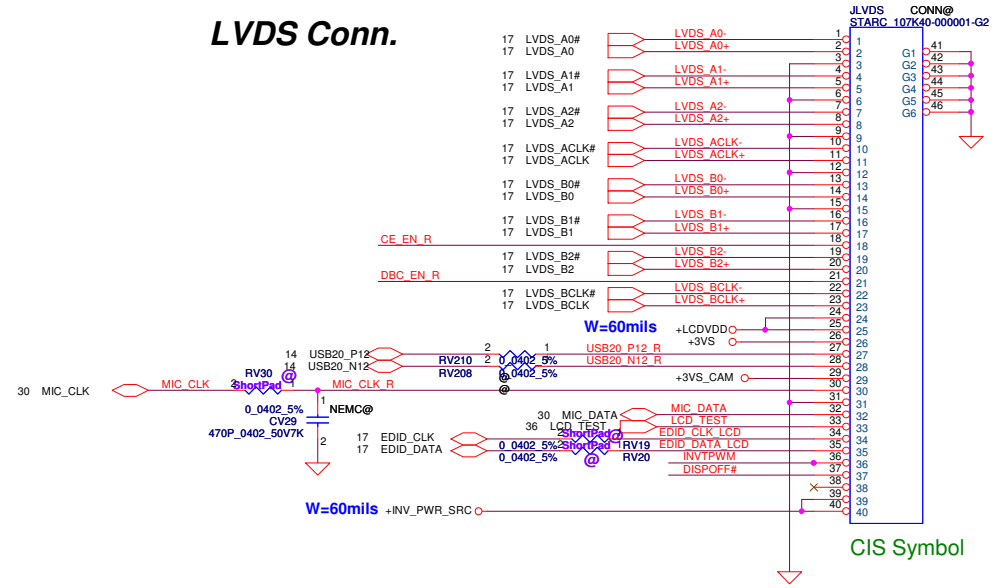
LCD backlight PWR CTRL



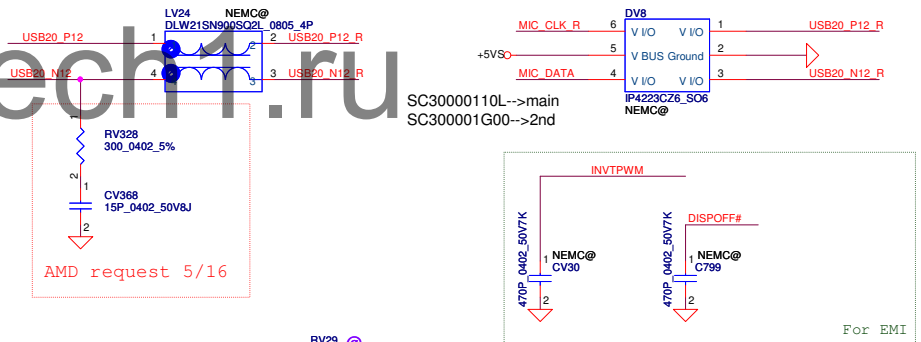
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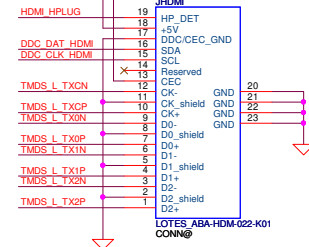
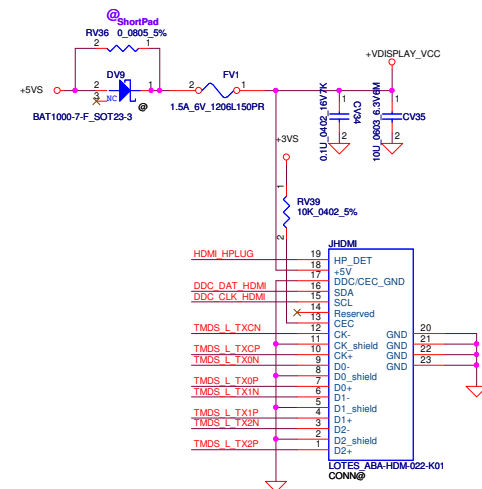
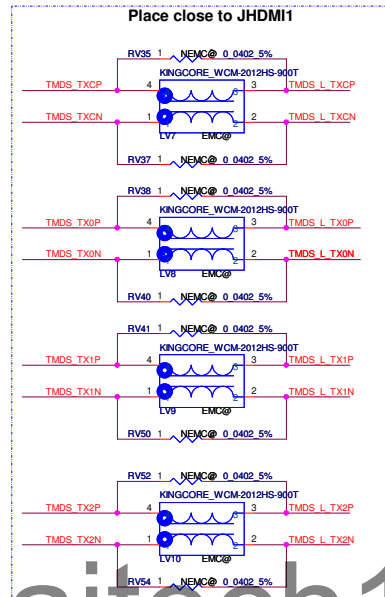
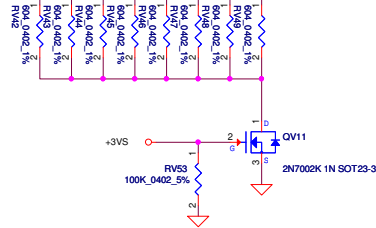
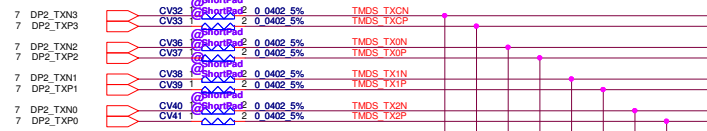
LVDS Conn.



* Reserved for EMI/ESD/RF
need to close to JLVDS



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				LA-9103P	
				Date: Wednesday, July 10, 2013	Sheet 18 of 52



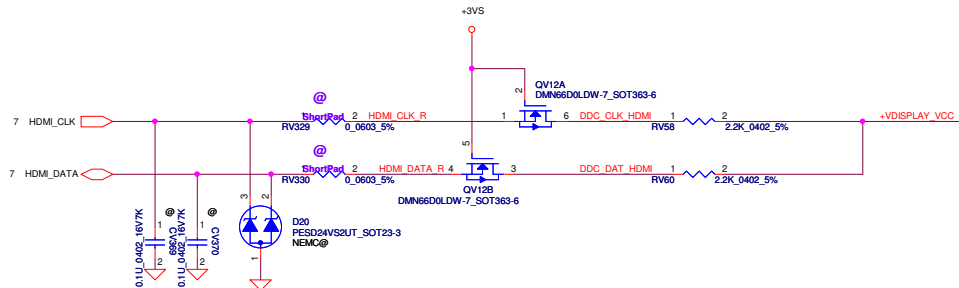
Part Number	Description
R000000023M	HDMI W/Logo:R000000023M

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TMD5_TXCP	NEMC@RV360	1	2	1P_0402_50V8J
TMD5_TXON	NEMC@RV362	1	2	1P_0402_50V8J
TMD5_TXOP	NEMC@RV363	1	2	1P_0402_50V8J
TMD5_TXIN	NEMC@RV365	1	2	1P_0402_50V8J
TMD5_TXIP	NEMC@RV367	1	2	1P_0402_50V8J
TMD5_TX2N	NEMC@RV361	1	2	1P_0402_50V8J
TMD5_TX2P	NEMC@RV364	1	2	1P_0402_50V8J

TMD5_L_TXCN	CV349	1	2	1P_0402_50V8J
TMD5_L_TXCP	CV350	1	2	1P_0402_50V8J
TMD5_L_TXON	CV351	1	2	1P_0402_50V8J
TMD5_L_TXOP	CV352	1	2	1P_0402_50V8J
TMD5_L_TXIN	CV353	1	2	1P_0402_50V8J
TMD5_L_TXIP	CV354	1	2	1P_0402_50V8J
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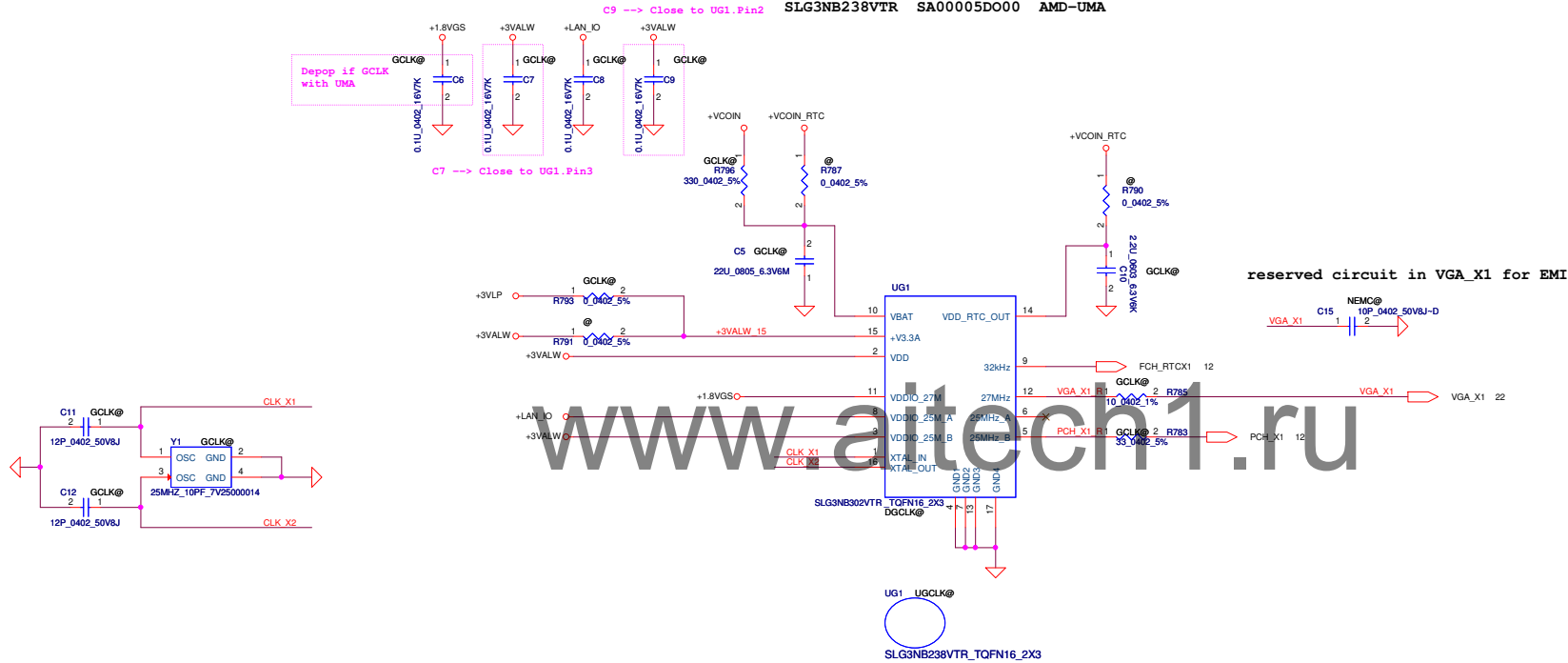
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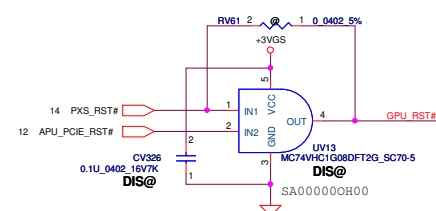
CV365, CV367
Please close APU side

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		Date	Wednesday, July 10, 2013
		Sheet	19 of 52

SLG3NB244VTR SA000057I00 Intel-UMA
SLG3NB300VTR SA00005RS00 Intel-DIS
SLG3NB302VTR SA00006D500 AMD-DIS
SLG3NB238VTR SA00005D000 AMD-UMA



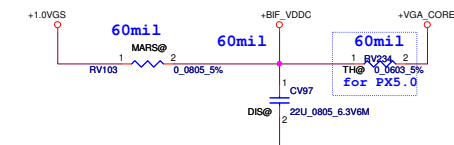
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	GCLK	
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				LA-9103P	1.0
				Date: Wednesday, July 10, 2013	Sheet 20 of 52



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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	ATI ThamesXT M2 PCIE/LVDS	
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Date	Wednesday, July 10, 2013	Sheet	21	of	50	

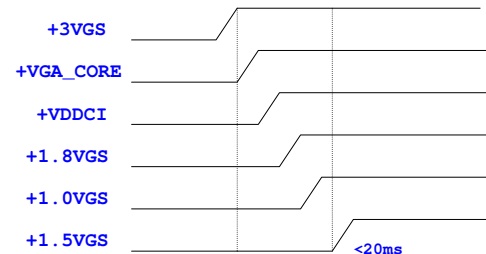
Switch circuits in BACO desings for Thanes/Seymour only

for PX4.0 and PX5.0



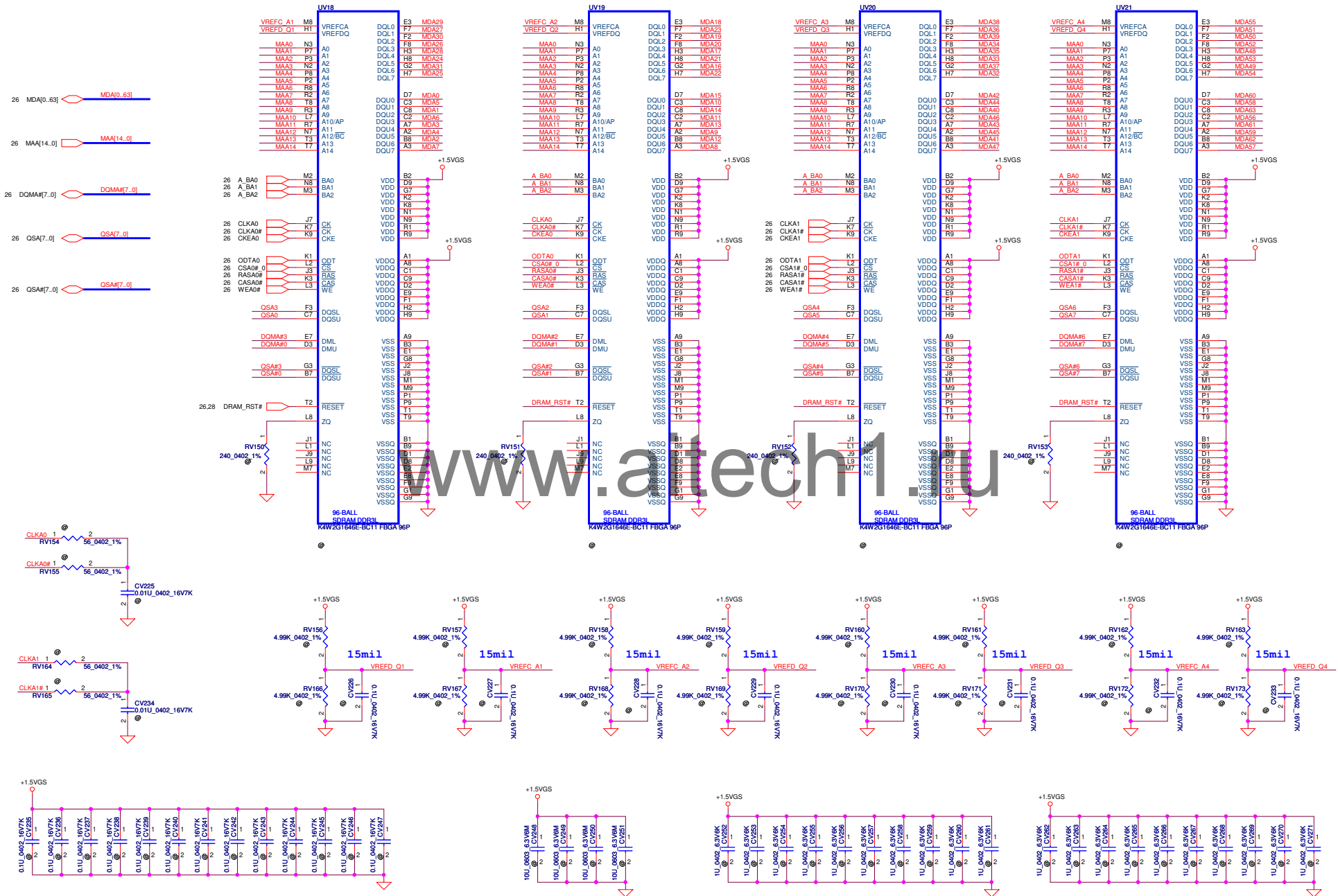
The schematic diagram illustrates the power supply section of the ADXL345 evaluation board. It features two voltage regulators: a 5V regulator (QV22, AP2301GN+HF, SOT23-3) and a 3.3V regulator (QV23, 2N7002K, SOT23-3). The 5V regulator is powered by a 5V input (5VALW) and provides a 5V output (5VOUT). The 3.3V regulator is powered by a 3.3V input (3V3W) and provides a 3.3V output (3V3OUT). Both regulators have decoupling capacitors (CV101, CV102, CV103) and input/output capacitors (RV107, RV108, RV109, RV110). The output of the 5V regulator is connected to the 5V pin of the ADXL345, and the output of the 3.3V regulator is connected to the 3.3V pin of the ADXL345. The schematic also shows the connection of the PXS_PWREN# signal to the PXS_PWREN pin of the ADXL345.

Power Sequence of Thames and Chelsea



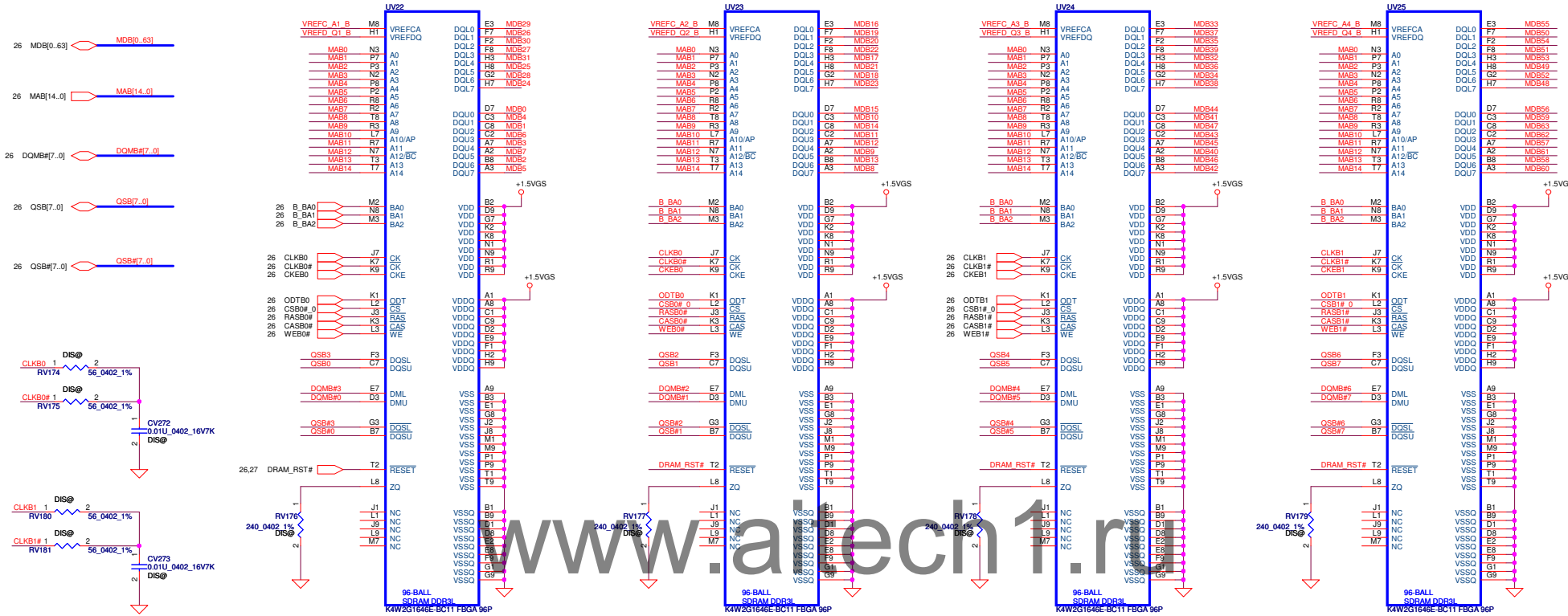
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	ATI ThamesXT M2 BACO POWER	
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				Date:	Wednesday, July 10, 2013	Sheet 23 of 50

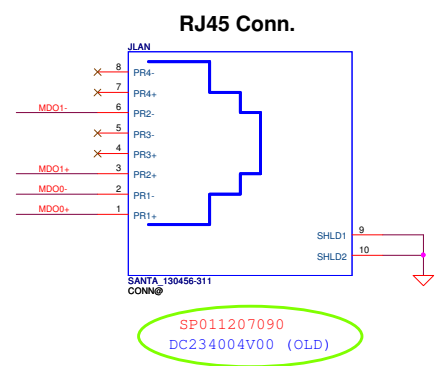
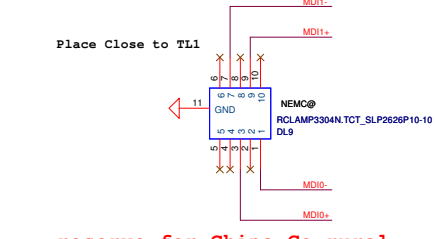
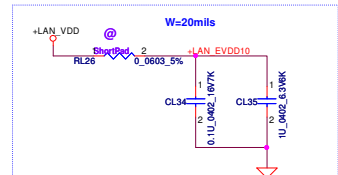
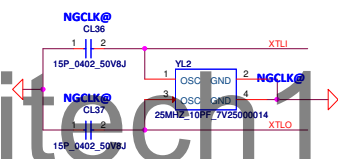
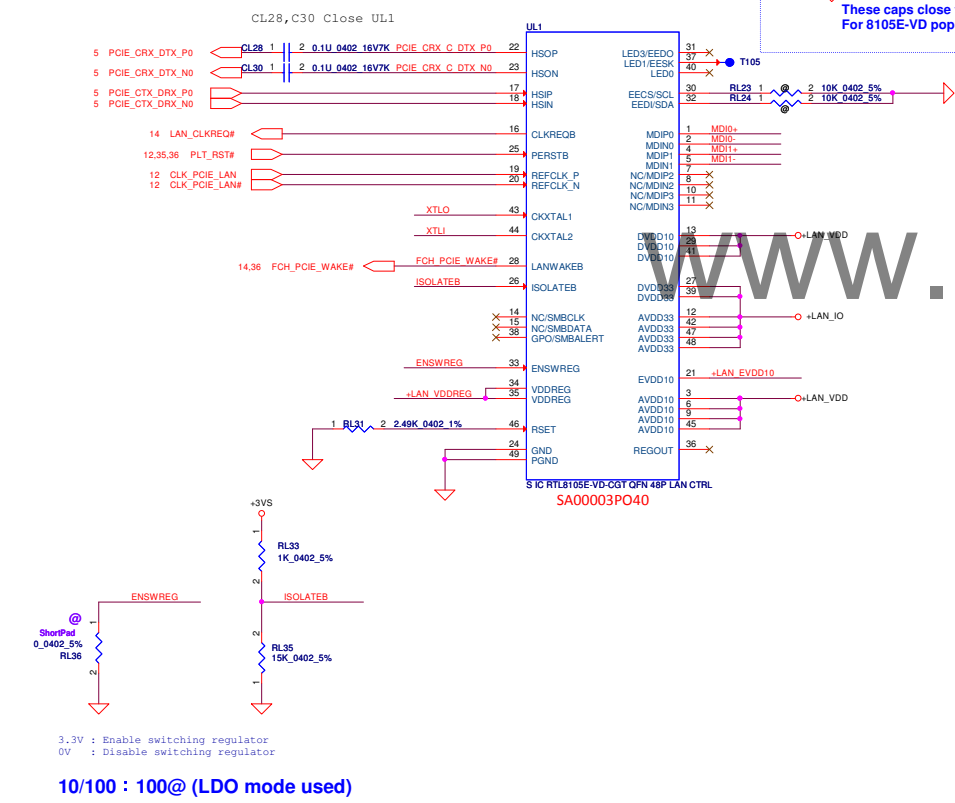
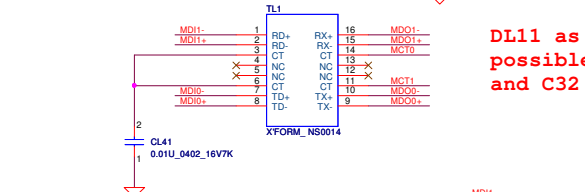
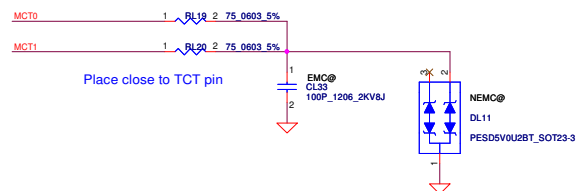
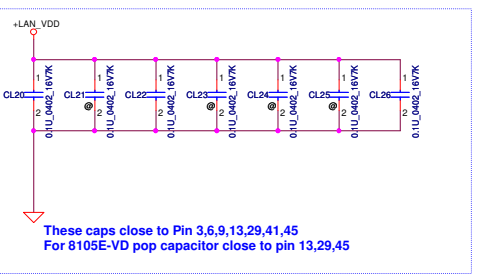
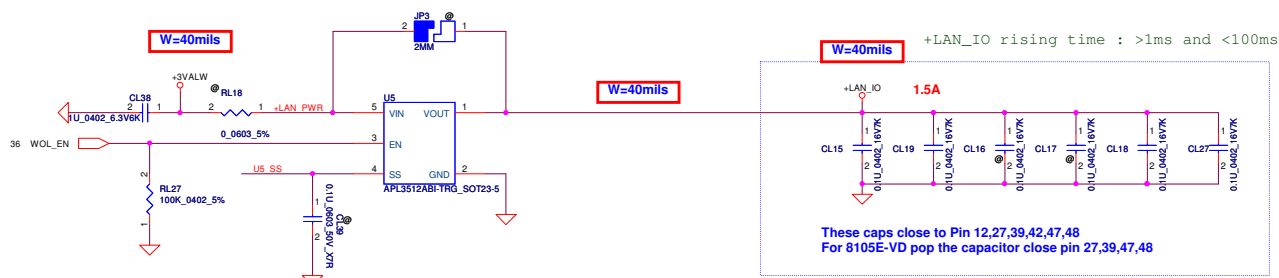
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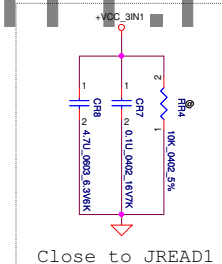
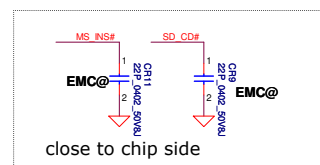
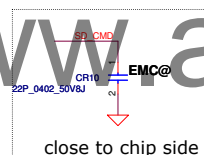
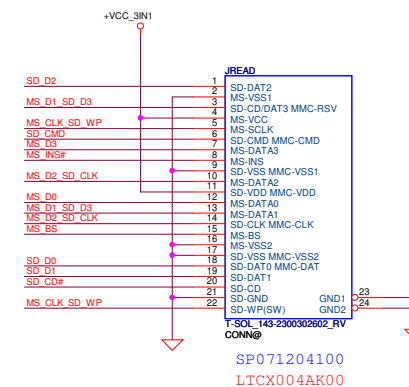
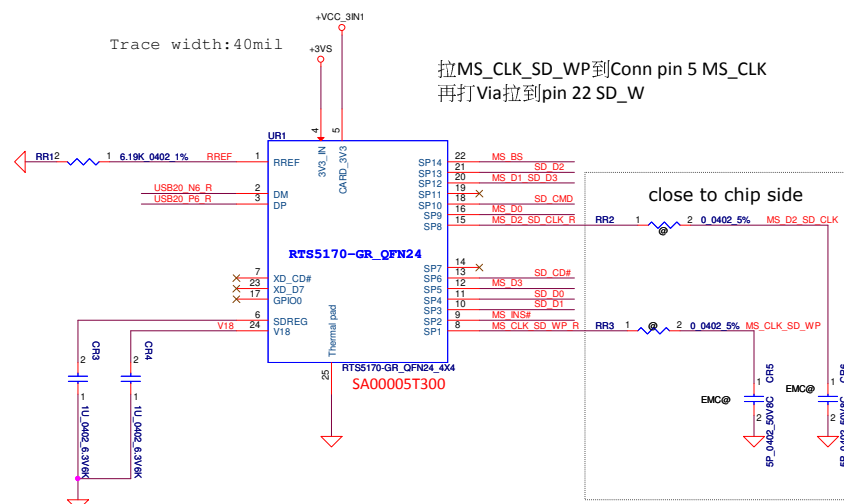
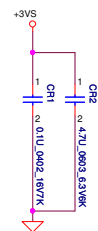
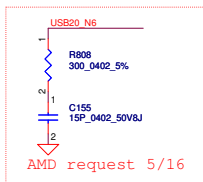
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						ATI ThamesXT M2 VRAM A				
						Size	Document Number			
		LA-9103P				Rev 1.0				
Date:		Wednesday, July 10, 2013			Sheet	27 of 50				

CHANNEL B : 256MB/512MB DDR3



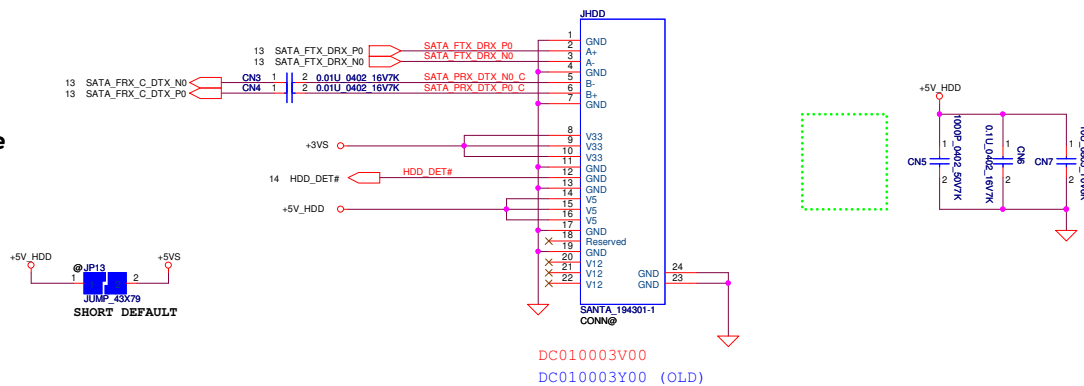


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				LA-9103P	Rev 1.0
				Date	Wednesday, July 10, 2013
				Sheet	29 of 52



SATA HDD Conn.

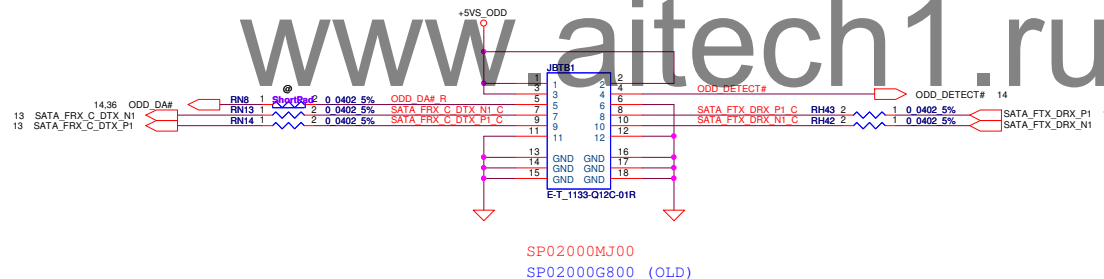
+5V_HDD Source



ODD BTB Conn.

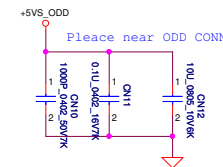
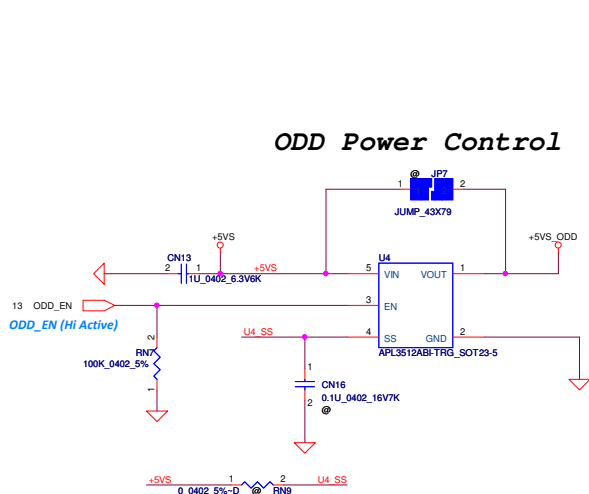
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RX

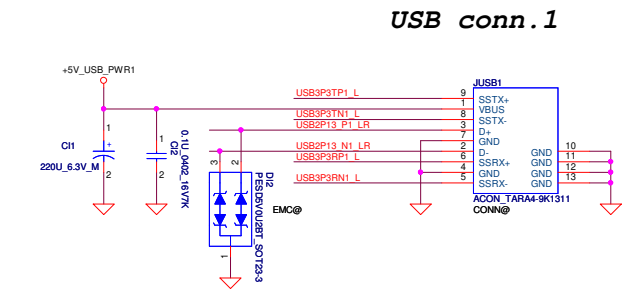
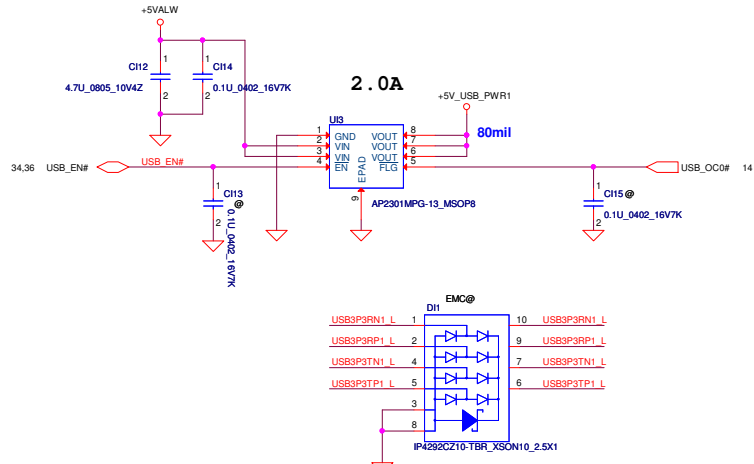
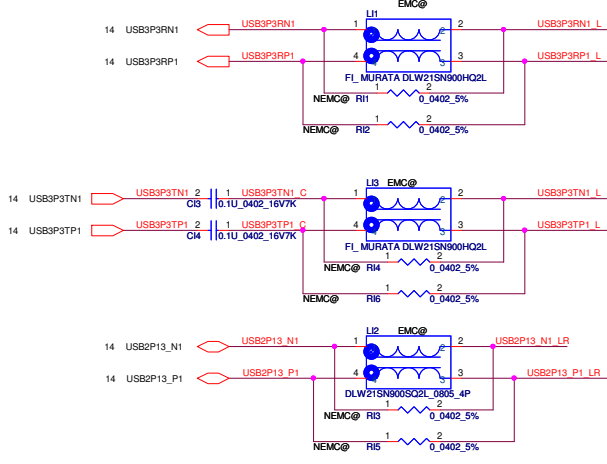


TX

ODD Power Control

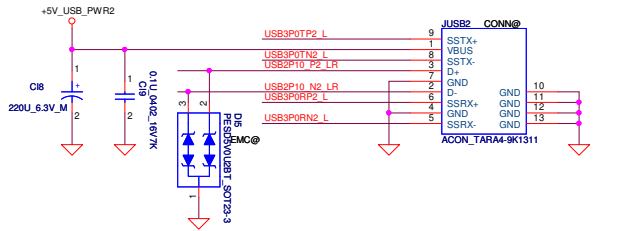
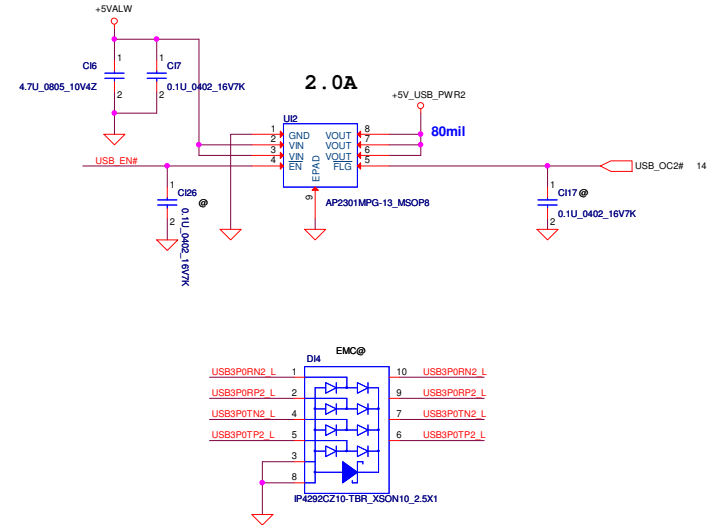
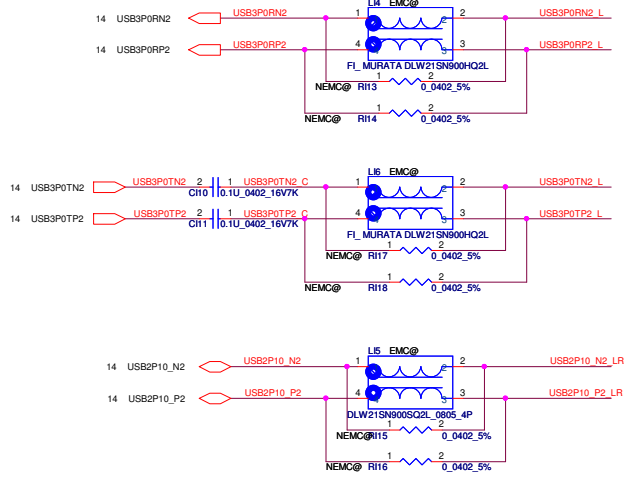


9/20 OAK Intel USB3.0 issue
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To SM070000S80 (S COM FL_CHENG HANN WCM2012F2SF-670T04)
1/22 Change LI1, LI3, LI4, LI6 Part
PN: from SM070000S80 (S COM FL_CHENG HANN WCM2012F2SF-670T04)
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To SM070001S00 (S COM FL_KINGCORE WCM-2012HS-900T)-2nd

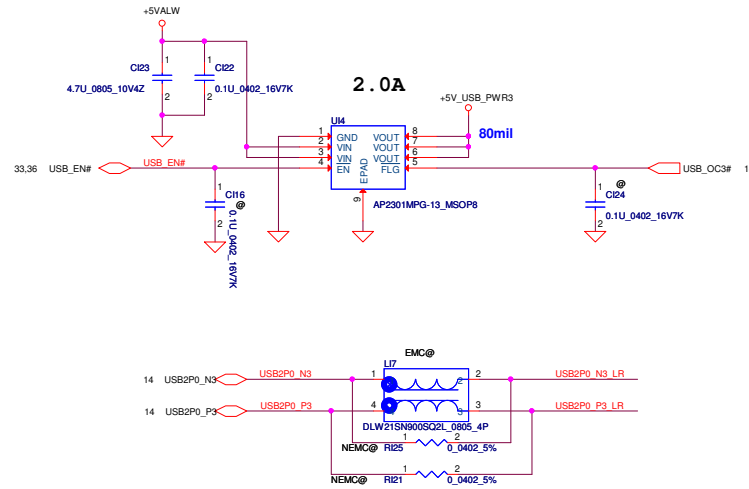


USB conn.1

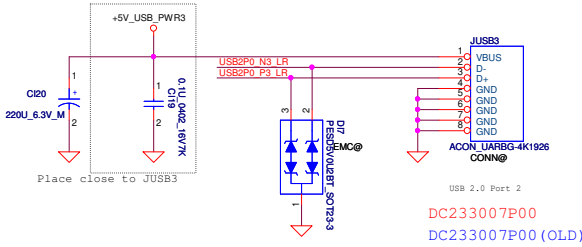
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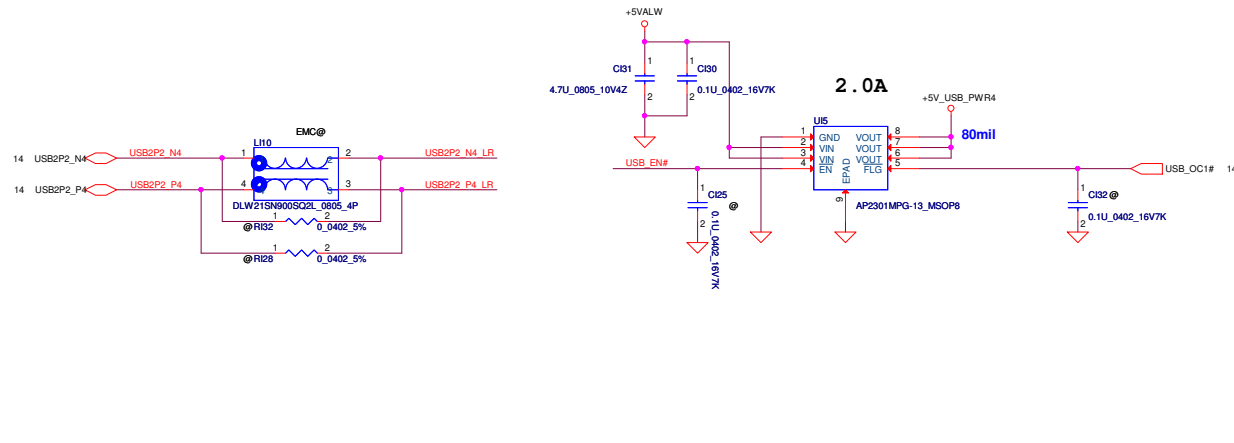
USB conn.2



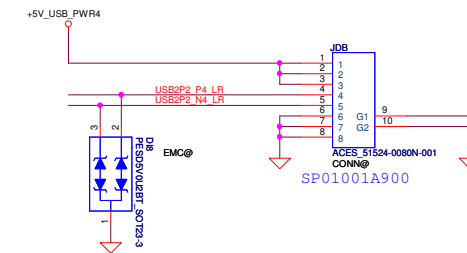
USB conn. 3



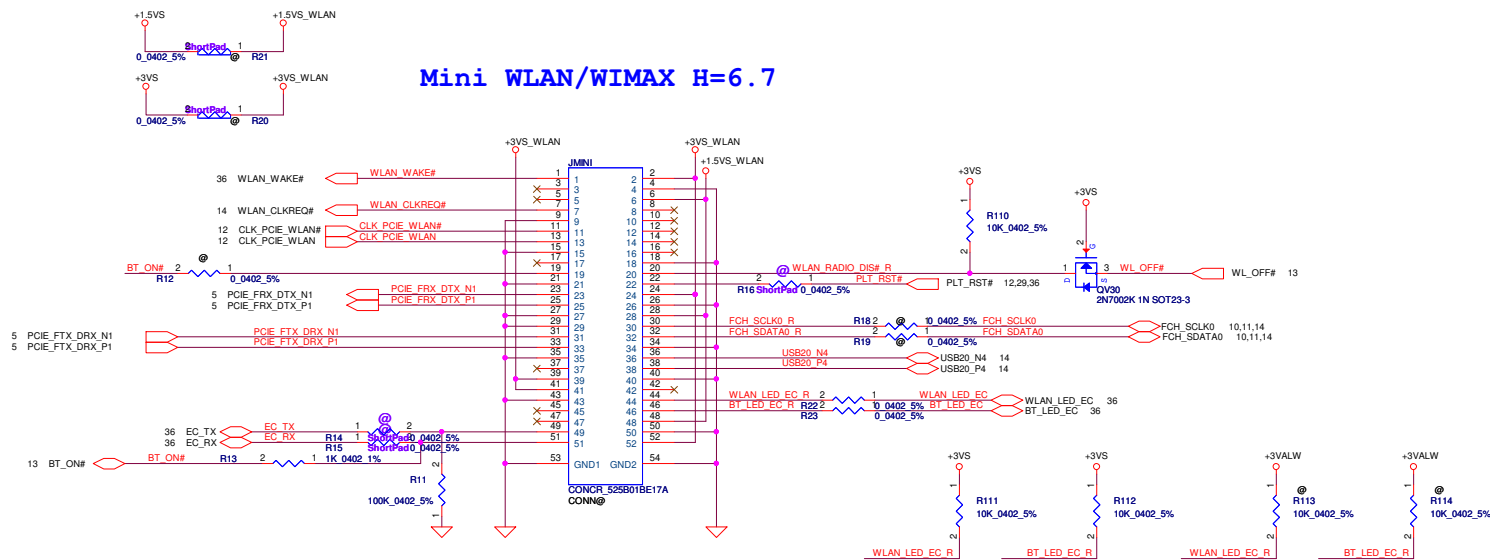
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USB conn. 4



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				LA-9103P	1.0
				Date: Wednesday, July 10, 2013	Sheet 34 of 52



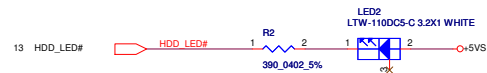
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CC47靠近wlan connector

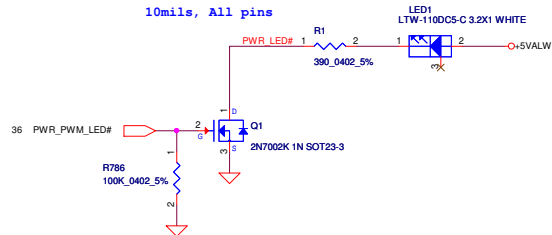
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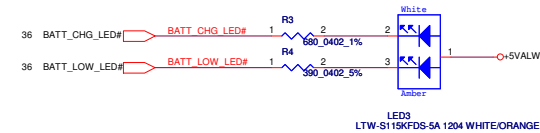
HDD LED



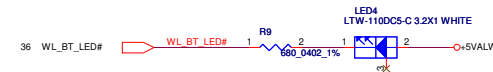
Power LED



Battery LED

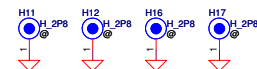
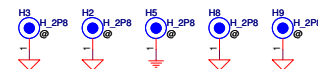


Wireless LED

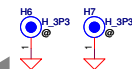
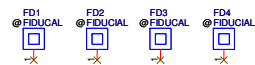


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				Date	Wednesday, July 10, 2013
				Sheet	35 of 52
				Rev	1.0

Screw Hole



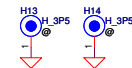
APU Screw Hole



GPU Screw Hole



FAN Screw Hole



ODD Screw Hole

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				Date	Wednesday, July 10, 2013
				Sheet	37 of 52
				Rev	1.0

TOP Side

SW1
SMT1-05-A 4P

CE20
0.1uF 16V7K

100K 0402 5%

ON/OFF

Bottom Side

SW2
SMT1-05-A 4P

Pop only for
SSI debug

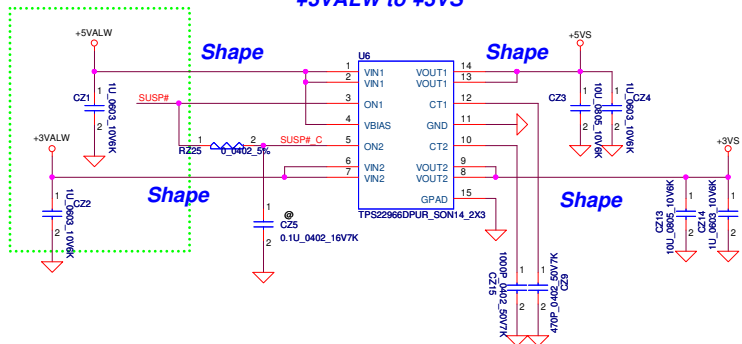
The top diagram illustrates the EN_DFAN1 control circuit. It includes a +5V supply connected to a 2.2uF 6.3V8K capacitor (CE22) and a 100uF 0.402 50V7K capacitor (CE23). A 40mil trace connects the output of CE22 to the EN_DFAN1 pin. The bottom diagram illustrates the FAN_SPEED1 control circuit. It includes a +5V supply connected to a 10K 0.402 5% resistor (RE50) and a 0.01uF 0.402 16V7K capacitor (CE24). A 40mil trace connects the output of CE24 to the FAN_SPEED1 pin. Both diagrams also show a +FAN_POWER input connected to the fan control IC.

[illegible][illegible]

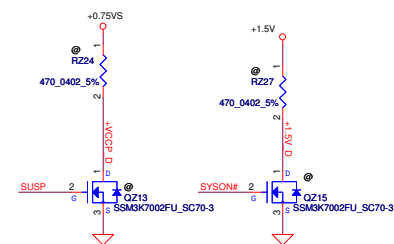
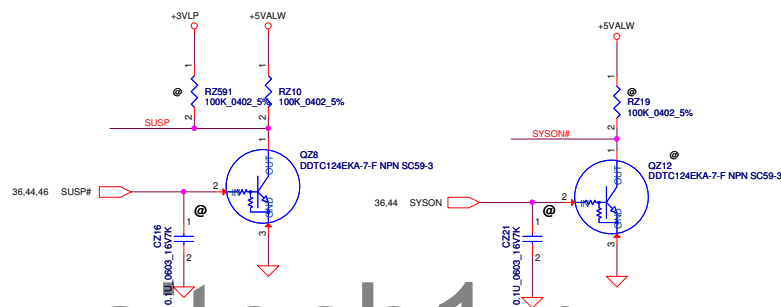
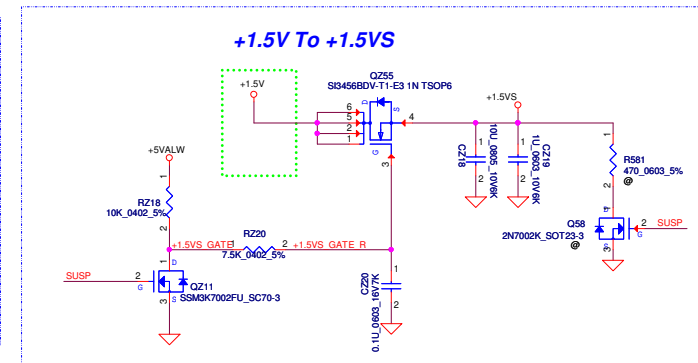
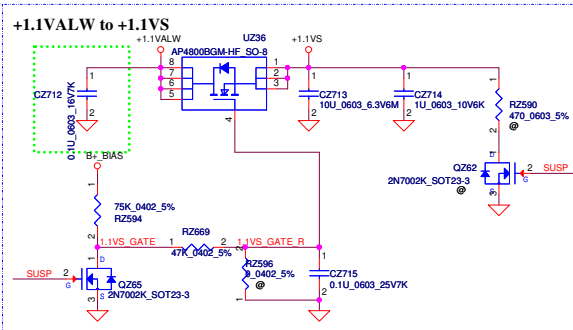
The schematic diagram illustrates the LED driver circuit. It features two input power rails: +5VS and +5VS_KBL. The +5VS rail is connected to a 0.75A_24V_1812.075-24DR LED strip. The +5VS_KBL rail is connected to a 100_0A003.83V0A LED strip. The circuit includes a 20mOhm resistor (FE1) and a 0.0805_5% resistor (RE58) in series with the LED strips. A 10K_0402_5% resistor (RE59) is connected to the +3VS rail. The circuit also includes a 2N7002BKW_SOT323-3 MOSFET (QE4) and a 3IX4568DV-T1-E3 1N TSOP6 MOSFET (QE5). The output of the circuit is connected to the LED strips via a 100_0A003.83V0A LED strip and a 100_0A003.83V0A LED strip. The circuit is powered by a 3V battery (3V) and a 5V battery (5V).

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				LA-9103P	
Date: Wednesday, July 10, 2013		Sheet 36 of 50			

+5VALW to +5VS
+3VALW to +3VS



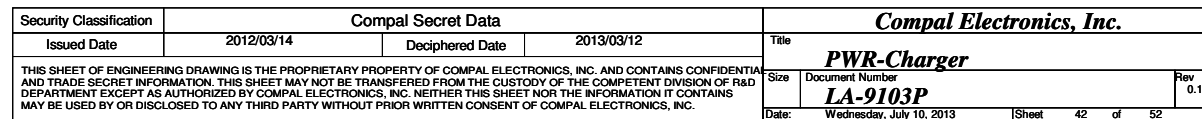
CTx (pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



Page 1

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				Date:	Wednesday, July 10, 2013	Sheet 40 of 50



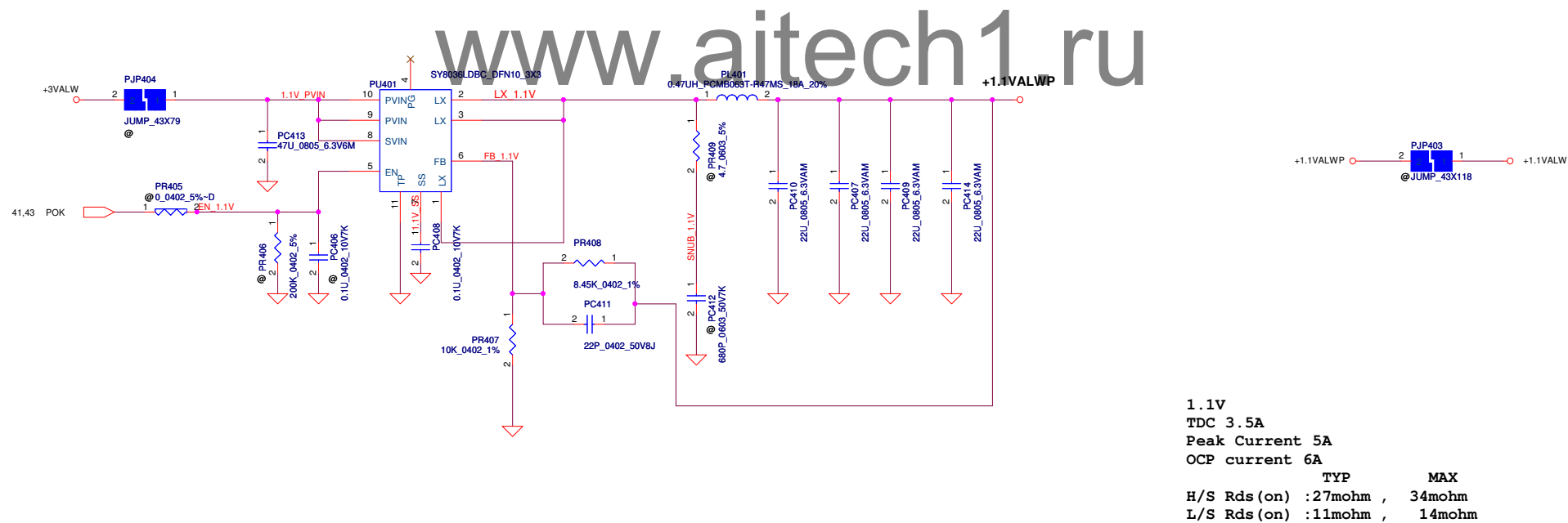
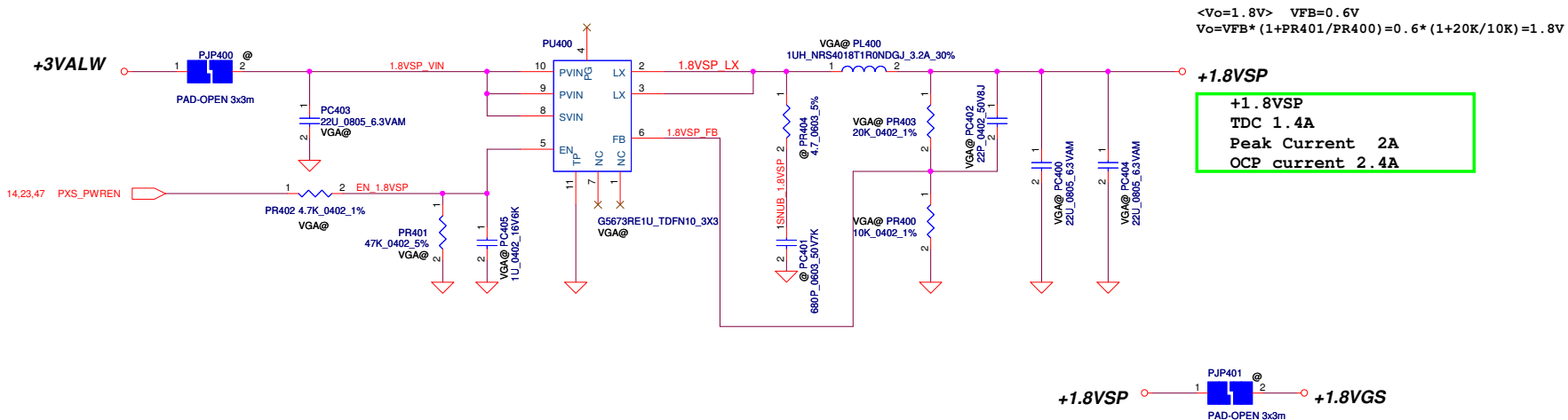
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1.5VP
TDC 11A
Peak Current 16A
OCP current 19A
TYP MAX
H/S Rds(on) : 23.2mohm , 27.8mohm
L/S Rds(on) : 7mohm , 8.4mohm

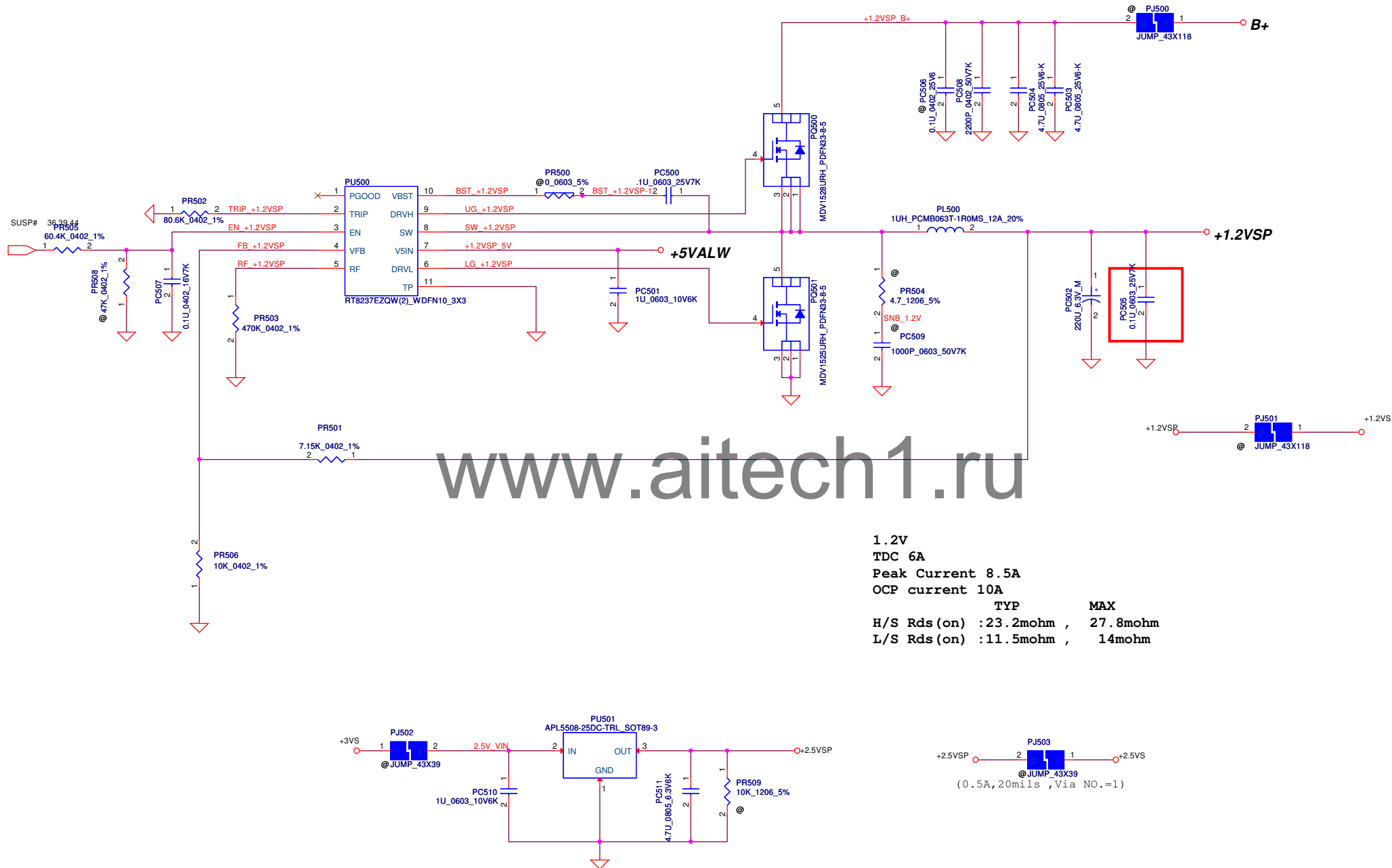
0.75VSP
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

+1.5VGPU
TDC 5.6A
Peak Current 8A
OCP current 9.6A

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				Date	Wednesday, July 10, 2013
				Sheet	44 of 52

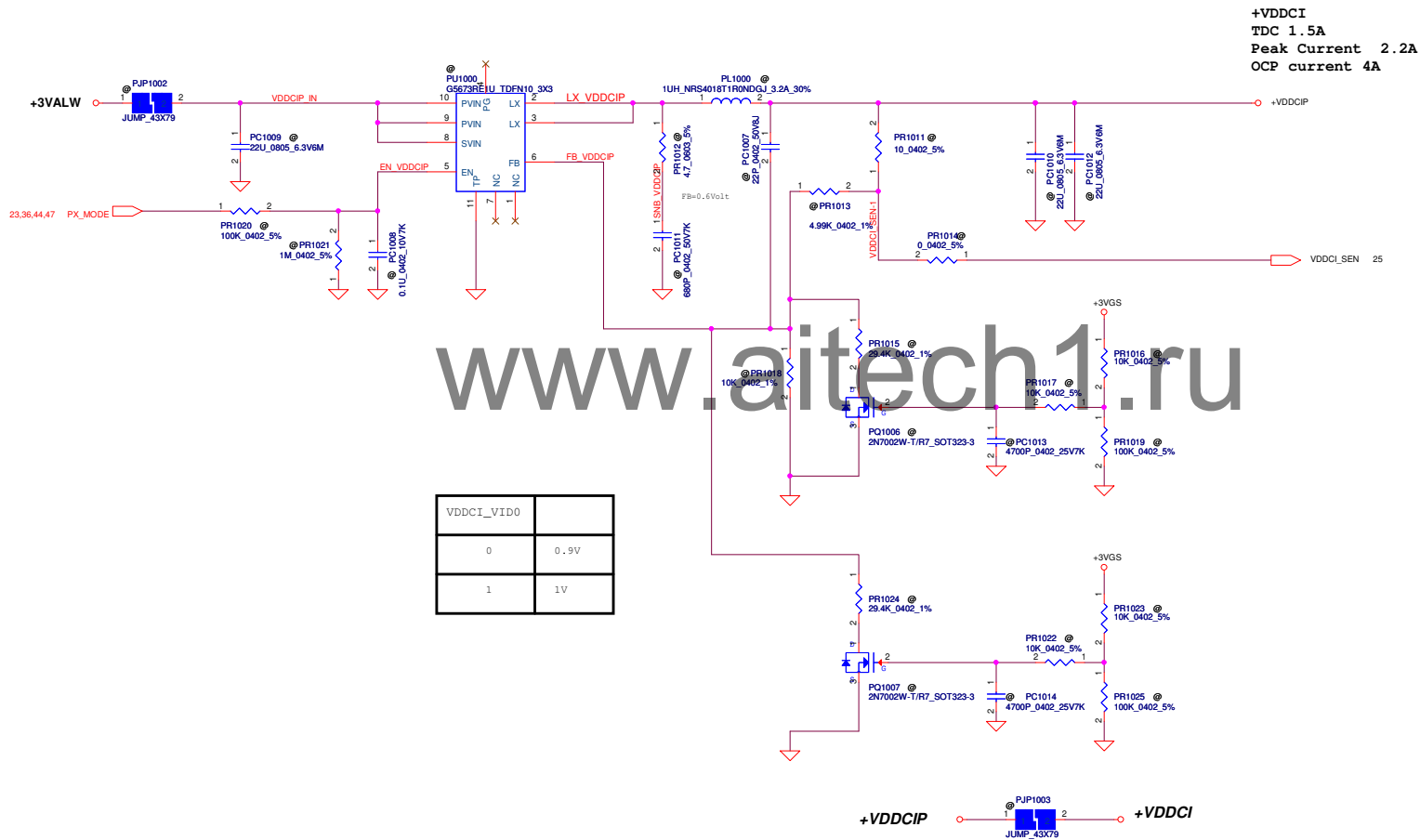


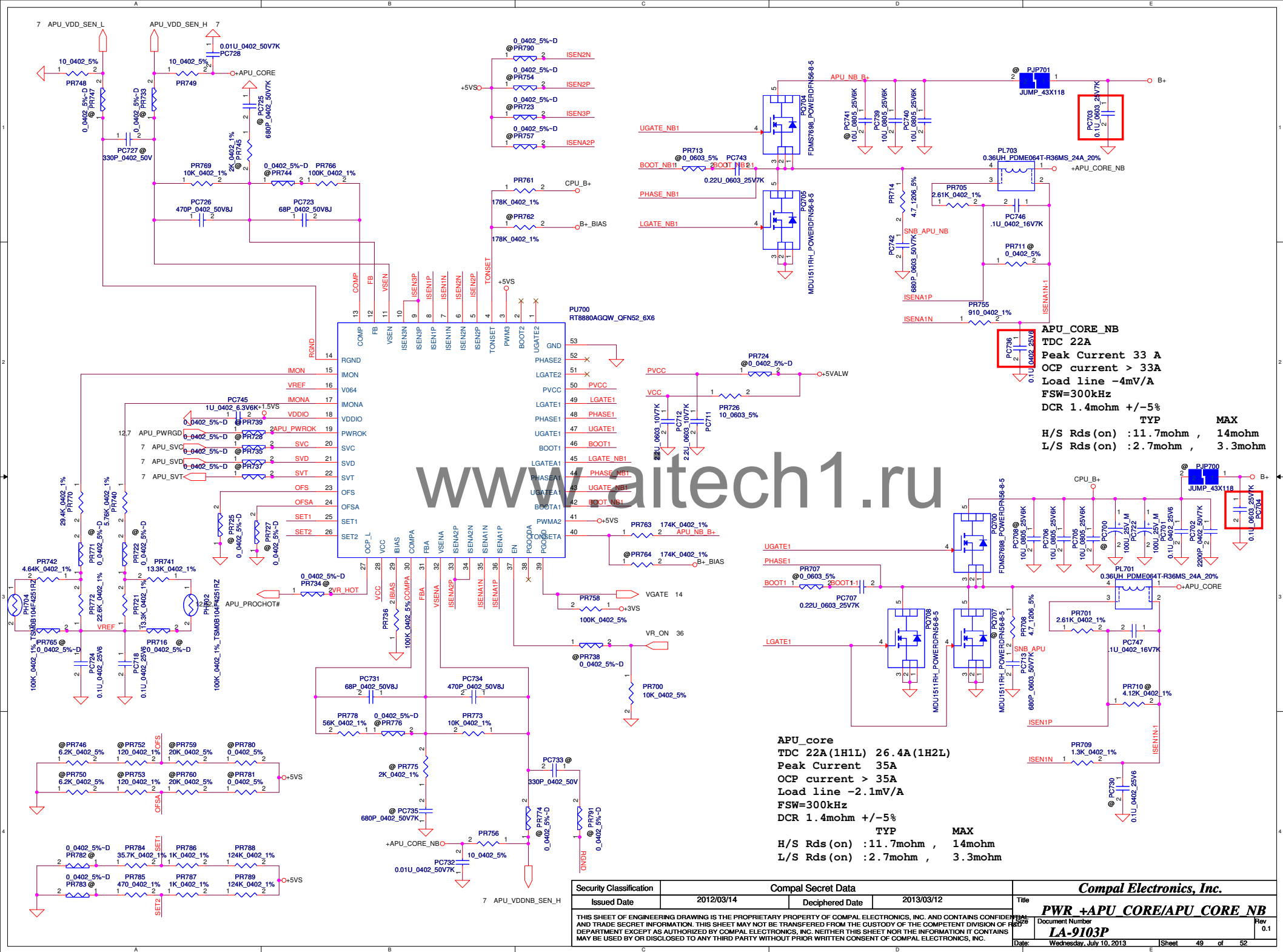
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/03/14	Deciphered Date	2013/03/12	Title	PWR-1.8VSP/1.1VALWP
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				LA-9103P	Rev 0.1
				Date: Wednesday, July 10, 2013	Sheet 45 of 52



1.2V
 TDC 6A
 Peak Current 8.5A
 OCP current 10A
 TYP MAX
 H/S Rds (on) : 23.2mohm , 27.8mohm
 L/S Rds (on) : 11.5mohm , 14mohm

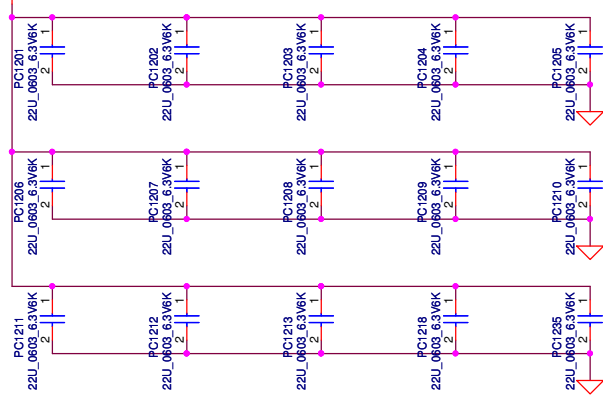
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Size		Document Number		Rev	
		LA-9103P		0.1	
Date		Wednesday, July 10, 2013		Sheet 46 of 52	



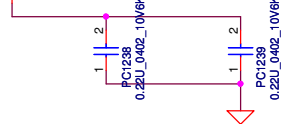


+APU_CORE

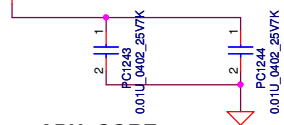
+APU_CORE



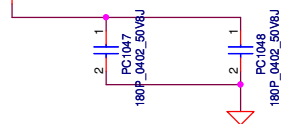
+APU_CORE



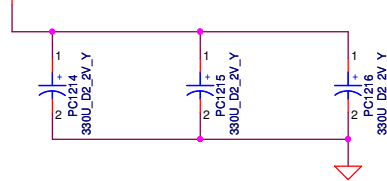
+APU_CORE



+APU_CORE

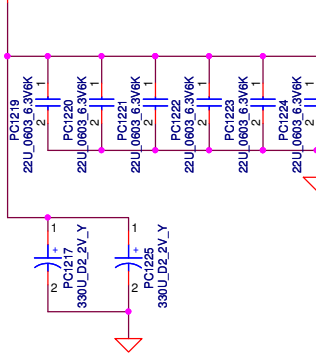


+APU_CORE



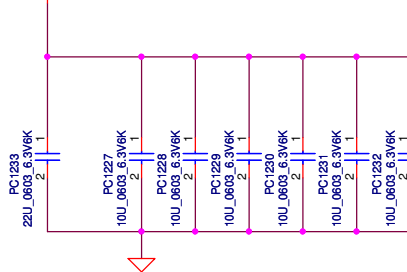
+APU_CORE_NB

+APU_CORE_NB



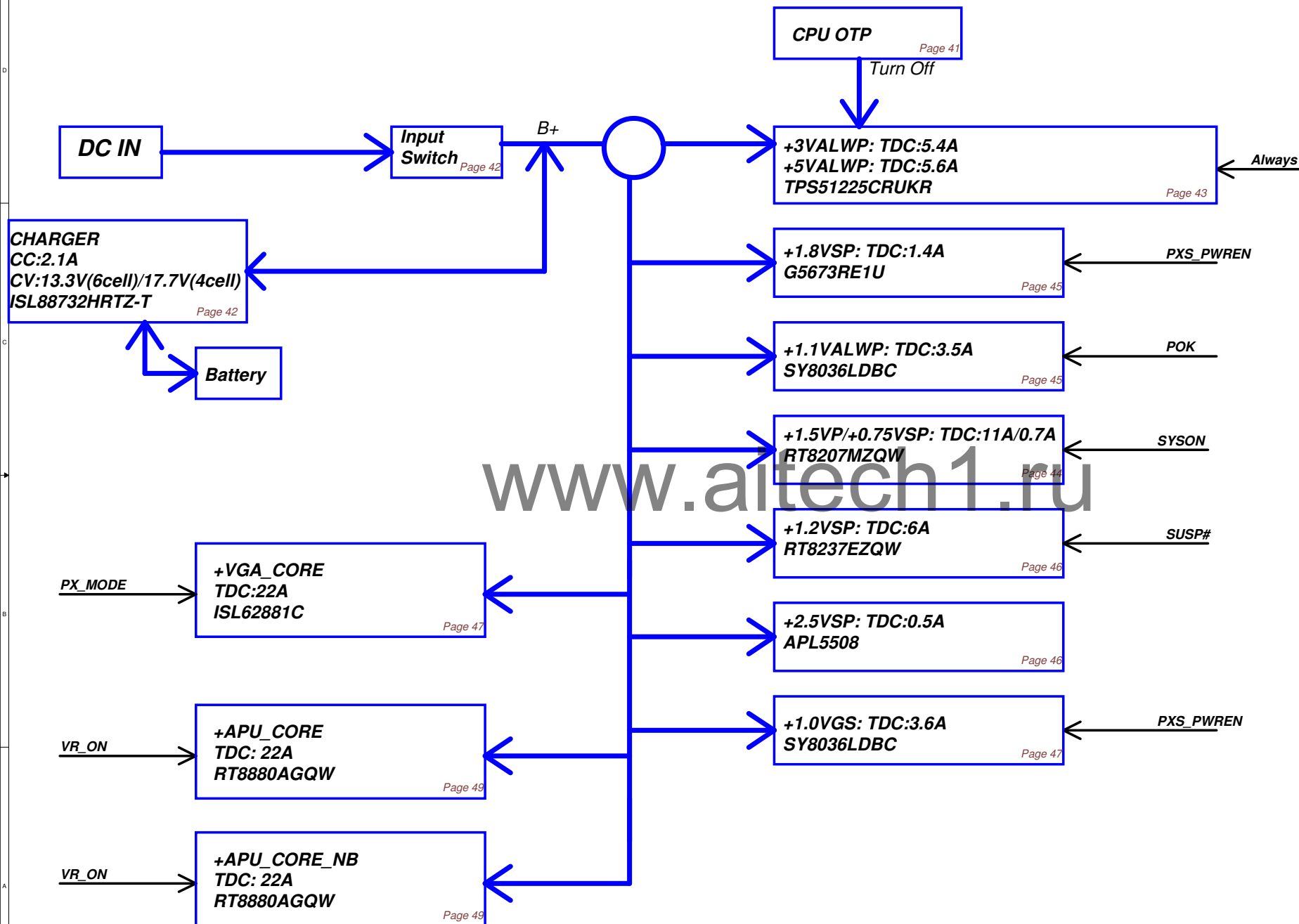
+1.2VS

+1.2VS



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Size	Document Number	Rev		0.1	
Date	Wednesday, July 10, 2013	Sheet	50	of	52

Power block



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				Date	Wednesday, July 10, 2013
				Sheet	51 of 52

Page 1

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				LA-9103P	
Date:	Wednesday, July 10, 2013	Sheet	52	of	52